1. Record Nr. UNISANNIOBVEE018443

Autore	Botero, Giovanni
Titolo	Della ragione di stato, libri dieci. Di Giouanni Botero Benese, reuisti dall'autore, e arricchiti in piÃ¹ luoghi di discorsi, e di cose memorabili. ... Tre libri della grandezza della cittÃ , del medesimo autore
Pubbl/distr/stampa	In Roma : presso Vincenzio Pellagallo, 1590 ((In Roma) : appresso Giacomo Ruffinelli, 1590
Descrizione fisica	\4!, 400, \12! p. : ill. ; 8Âº
Collocazione	GEA 1 0017
Lingua di pubblicazione	Italiano
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Tre libri della grandezza delle cittÃ inizia con proprio front. a c. X1 Cors. ; rom Segn.: ÏÂ²A-2Bâ¸2Câ¶ Vignetta xil. sul front.

2. Record Nr. UNINA9910483523303321

Titolo	Automated Technology for Verification and Analysis : 4th International Symposium, ATVA 2006, Beijing, China, October 23-26, 2006, Proceedings / / edited by Susanne Graf, Wenhui Zhang
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2006
ISBN	3-540-47238-X
Edizione	[1st ed. 2006.]
Descrizione fisica	1 online resource (XIV, 546 p.)
Collana	Programming and Software Engineering, , 2945-9168 ; ; 4218
Altri autori (Persone)	GrafSusanne ZhangWenhui <1963->
Disciplina	004.01/5113
Soggetti	Computer-aided engineering Computer science Computer networks Computers, Special purpose Software engineering Computer-Aided Engineering (CAD, CAE) and Design Computer Science Logic and Foundations of Programming Computer Communication Networks Special Purpose and Application-Based Systems Software Engineering
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Keynote Speeches -- Analysis of Recursive Probabilistic Models -- Verification Challenges and Opportunities in the New Era of Microprocessor Design -- Automated Abstraction of Software -- Regular Papers -- Symmetry Reduction for Probabilistic Model Checking Using Generic Representatives -- Eager Markov Chains -- A Probabilistic Learning Approach for Counterexample Guided Abstraction Refinement -- A Fine-Grained Fullness-Guided Chaining Heuristic for Symbolic Reachability Analysis -- Model Checking Timed Systems with Urgencies -- Whodunit? Causal Analysis for Counterexamples -- On the Membership Problem for Visibly Pushdown Languages -- On the Construction of Fine Automata for Safety

Properties -- On the Succinctness of Nondeterminism -- Efficient Algorithms for Alternating Pushdown Systems with an Application to the Computation of Certificate Chains -- Compositional Reasoning for Hardware/Software Co-verification -- Learning-Based Symbolic Assume-Guarantee Reasoning with Automatic Decomposition -- On the Satisfiability of Modular Arithmetic Formulae -- Selective Approaches for Solving Weak Games -- Controller Synthesis and Ordinal Automata -- Effective Contraction of Timed STGs for Decomposition Based Timed Circuit Synthesis -- Synthesis for Probabilistic Environments -- Branching-Time Property Preservation Between Real-Time Systems -- Automatic Verification of Hybrid Systems with Large Discrete State Space -- Timed Unfoldings for Networks of Timed Automata -- Symbolic Unfoldings for Networks of Timed Automata -- Ranked Predicate Abstraction for Branching Time: Complete, Incremental, and Precise -- Timed Temporal Logics for Abstracting Transient States -- Predicate Abstraction of Programs with Non-linear Computation -- A Fresh Look at Testing for Asynchronous Communication -- Proactive Leader Election in Asynchronous Shared Memory Systems -- A Semantic Framework for Test Coverage -- Monotonic Set-Extended Prefix Rewriting and Verification of Recursive Ping-Pong Protocols -- Analyzing Security Protocols in Hierarchical Networks -- Functional Analysis of a Real-Time Protocol for Networked Control Systems -- Symbolic Semantics for the Verification of Security Properties of Mobile Petri Nets -- Sigref – A Symbolic Bisimulation Tool Box -- Towards a Model-Checker for Counter Systems -- The Implementation of Mazurkiewicz Traces in POEM -- Model-Based Tool-Chain Infrastructure for Automated Analysis of Embedded Systems.

Sommario/riassunto

The Automated Technology for Veri?cation and Analysis (ATVA) international symposium series was initiated in 2003, responding to a growing interest in formal veri?cation spurred by the booming IT industry, particularly hardware design and manufacturing in East Asia. Its purpose is to promote research on automated veri?cation and analysis in the region by providing a forum for int- action between the regional and the international research/industrial commu- ties of the ? eld. ATVA 2006, the fourth of the ATVA series, was held in Beijing, China, October 23-26, 2006. The main topics of the symposium include th- ries useful for providing designers with automated support for obtaining correct software or hardware systems, as well as the implementation of such theories in tools or their application. This year, we received a record number of papers: a total of 137 submissions from 27 countries. Each submission was assigned to three Program Comm- tee members, who could request help from subreviewers, for rigorous and fair evaluation. The ?nal deliberation by the Program Committee was conducted through Springer’s Online Conference Service for a duration of about 10 days after nearly all review reports had been collected. In the end, 35 papers were selected for inclusion in the program. ATVA 2006 had three keynote speeches given respectively by Thomas Ball, Jin Yang, and Mihalis Yannakakis. The main symposium was preceded by a tutorial day, consisting of three two-hourlectures given by the keynotespeakers.