1. Record Nr. UNISALENTO991004072169707536

Autore	Poulouin, Gérard
Titolo	C.F. Ramuz : oeuvres et critique 1982-1988 : et compléments 1921-1929 à la bibliographie Bringolf-Verdan / par Gérard Poulouin
Pubbl/distr/stampa	Paris : Lettres Modernes, 1993
ISBN	2256909271
Descrizione fisica	1 v. ; 19 cm
Collana	Les carnets bibliographiques de la revue des lettres modernes
Altri autori (Persone)	Bringolf, Théophile Verdan, Jacques
Disciplina	843.912
Soggetti	Ramuz, Charles Ferdinand Bibliografia Ramuz, Charles Ferdinand Bibliografia
Lingua di pubblicazione	Francese
Formato	Materiale a stampa
Livello bibliografico	Monografia

2. Record Nr. UNINA9910437590403321

Titolo	Computer Engineering and Technology : 16th National Conference, NCCET 2012, Shanghai, China, August 17-19, 2012, Revised Selected Papers / / edited by Weixia Xu, Liquan Xiao, Pingjing Lu, Jinwen Li, Chengyi Zhang
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2013
ISBN	3-642-35898-5
Edizione	[1st ed. 2013.]
Descrizione fisica	1 online resource (XIV, 263 p. 164 illus.)
Collana	Communications in Computer and Information Science, , 1865-0937 ; ; 337
Disciplina	004.1
Soggetti	Microprocessors Computer architecture Computer arithmetic and logic units Computer storage devices Memory management (Computer science) Logic design Computers Processor Architectures Arithmetic and Logic Structures Computer Memory Structure Logic Design Hardware Performance and Reliability
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Session 1: Microprocessor and Implementation -- A Method of Balancing the Global Multi-mode Clock Network in Ultra-large Scale CPU -- Hardware Architecture for the Parallel Generation of Long-Period Random Numbers Using MT Method -- MGTE: A Multi-level Hybrid Verification Platform for a 16-Core Processer -- An Efficient Parallel SURF Algorithm for Multi-core Processor -- A Study of Cache Design in Stream Processor -- Design and Implementation of Dynamically Reconfigurable Token Coherence Protocol for Many-Core

Processor -- Dynamic and Online Task Scheduling Algorithm Based on Virtual Compute Group in Many-Core Architecture -- ADL and High Performance Processor Design -- Session 2: Design of Integration Circuit -- The Design of the ROHC Header Compression Accelerator -- A Hardware Implementation of Nussinov RNA Folding Algorithm -- A Configurable Architecture for 1-D Discrete Wavelet Transform -- A Comparison of Folded Architectures for the Discrete Wavelet Transform -- A High Performance DSP System with Fault Tolerant for Space Missions -- The Design and Realization of Campus Information Release Platform Based on Android Framework -- A Word-Length Optimized Hardware Gaussian Random Number Generator Based on the Box-Muller Method -- Session 3: I/O Interconnect -- DAMQ Sharing Scheme for Two Physical Channels in High Performance Router -- Design and Implementation of Dynamic Reliable Virtual Channel for Network-on-Chip -- HCCM: A Hierarchical Cross-Connected Mesh for Network on Chip -- Efficient Broadcast Scheme Based on Sub-network Partition for Many-Core CMPs on Gem5 Simulator -- A Quick Method for Mapping Cores Onto 2D-Mesh Based Networks on Chip -- Session 4: Measurement, Verification, and Others -- A Combined Hardware/Software Measurement for ARM Program Execution Time -- A Low-Complexity Parallel Two-Sided Jacobi Complex SVD Algorithm and Architecture for MIMO Beamforming Systems -- A Thermal-Aware Task Mapping Algorithm for Coarse Grain Reconfigurable Computing System -- DC Offset Mismatch Calibration for Time-Interleaved ADCs in High-Speed OFDM Receivers -- An Novel Graph Model for Loop Mapping on Coarse-Grained Reconfigurable Architectures -- Memristor Working Condition Analysis Based on SPICE Model -- On Stepsize of Fast Subspace Tracking Methods.

Sommario/riassunto

This book constitutes the refereed proceedings of the 16th National Conference on Computer Engineering and Technology, NCCET 2012, held in Shanghai, China, in August 2012. The 27 papers presented were carefully reviewed and selected from 108 submissions. They are organized in topical sections named: microprocessor and implementation; design of integration circuit; I/O interconnect; and measurement, verification, and others.