1.	Record Nr.	UNINA9910458608703321
	Titolo	VLSI test principles and architectures [[electronic resource]] : design for testability / / edited by Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen
	Pubbl/distr/stampa	Amsterdam ; ; Boston, : Elsevier Morgan Kaufmann Publishers, c2006
	ISBN	1-280-96684-X 9786610966844 0-08-047479-9
	Edizione	[1st edition]
	Descrizione fisica	1 online resource (809 p.)
	Collana	The Morgan Kaufmann series in systems on silicon
	Altri autori (Persone)	WangLaung-Terng WuCheng-Wen, EE Ph. D. WenXiaoqing
	Disciplina	621.39/5
	Soggetti	Integrated circuits - Very large scale integration - Testing Integrated circuits - Very large scale integration - Design Electronic books.
	Lingua di pubblicazione	Inglese
	Formato	Materiale a stampa
	Livello bibliografico	Monografia
	Note generali	Description based upon print version of record.
	Nota di bibliografia	Includes bibliographical references and index.
	Nota di contenuto	Front cover; Title page; Copyright page; Table of contents; Preface; In the Classroom; Acknowledgments; Contributors; About the Editors; 1 Introduction; Importance of Testing; Testing During the VLSI Lifecycle; VLSI Development Process; Design Verification; Yield and Reject Rate; Electronic System Manufacturing Process; System-Level Operation; Challenges in VLSI Testing; Test Generation; Fault Models; Stuck-At Faults; Transistor Faults; Open and Short Faults; Delay Faults and Crosstalk; Pattern Sensitivity and Coupling Faults; Analog Fault Models; Levels of Abstraction in VLSI Testing Register-Transfer Level and Behavioral Level Gate Level; Switch Level; Physical Level; Historical Review of VLSI Test Technology; Automatic Test Equipment; Automatic Test Pattern Generation; Fault Simulation; Digital Circuit Testing; Analog and Mixed-Signal Circuit Testing; Design for Testability; Board Testing; Boundary Scan Testing; Concluding Remarks; Exercises; Acknowledgments; References; 2 Design for Testability; Introduction; Testability Analysis; SCOAP Testability

Analysis; Combinational Controllability and Observability Calculation
Sequential Controllability and Observability Calculation Probability-Based Testability Analysis; Simulation-Based Testability Analysis; RTL Testability Analysis; Design for Testability Basics; Ad Hoc Approach; Test Point Insertion; Structured Approach; Scan Cell Designs; Muxed-D Scan Cell; Clocked-Scan Cell; LSSD Scan Cell; Scan Architectures; Full-Scan Design; Muxed-D Full-Scan Design; Clocked Full-Scan Design; LSSD Full-Scan Design; Partial-Scan Design; Random-Access Scan Design; Scan Design Rules; Tristate Buses; Bidirectional I/O Ports; Gated Clocks; Derived Clocks

Combinational Feedback Loops Asynchronous Set/Reset Signals; Scan Design Flow; Scan Design Rule Checking and Repair; Scan Synthesis; Scan Configuration; Scan Replacement; Scan Reordering; Scan Stitching; Scan Extraction; Scan Verification; Verifying the Scan Shift Operation; Verifying the Scan Capture Operation; Scan Design Costs; Special-Purpose Scan Designs; Enhanced Scan; Snapshot Scan; Error-Resilient Scan; RTL Design for Testability; RTL Scan Design Rule Checking and Repair; RTL Scan Synthesis; RTL Scan Extraction and Scan Verification; Concluding Remarks; Exercises; Acknowledgments

References 3 Logic and Fault Simulation; Introduction; Logic Simulation for Design Verification; Fault Simulation for Test and Diagnosis; Simulation Models; Gate-Level Network; Sequential Circuits; Logic Symbols; Unknown State u; High-Impedance State Z; Intermediate Logic States; Logic Element Evaluation; Truth Tables; Input Scanning; Input Counting; Parallel Gate Evaluation; Timing Models; Transport Delay; Inertial Delay; Wire Delay; Functional Element Delay Model; Logic Simulation; Compiled-Code Simulation; Logic Optimization; Logic Levelization; Code Generation; Event-Driven Simulation
Nominal-Delay Event-Driven Simulation

Sommario/riassunto	This book is a comprehensive guide to new DFT methods that will show the readers how to design a testable and quality product, drive down test cost, improve product quality and yield, and speed up time-to-market and time-to-volume.· Most up-to-date coverage of design for testability. · Coverage of industry practices commonly found in commercial DFT tools but not discussed in other books. · Numerous, practical examples in each chapter illustrating basic VLSI test principles and DFT architectures.· Lecture slides and exercise solutions for all chapters are now available.·

2. Record Nr.	UNISALENTO991003984149707536
Autore	Lorenzini, Roberto
Titolo	Attaccamento, conoscenza e disturbi di personalità / Roberto Lorenzini, Sandra Sassaroli
Pubbl/distr/stampa	Milano : R. Cortina, 1995
ISBN	8870783502
Descrizione fisica	VII, 197 p. ; 23 cm
Collana	Collana di psicologia clinica e psicoterapia
Altri autori (Persone)	Sassaroli, Sandraauthor
Disciplina	155.2
Soggetti	Personalità - Psicologia dello sviluppo
	Conoscenza - Psicologia dello sviluppo
Lingua di pubblicazione	Italiano
Formato	Materiale a stampa
Livello bibliografico	Monografia

3.	Record Nr.	UNINA9910703243703321
	Autore	Fleming Susan A
	Titolo	Motor carrier safety [[electronic resource]] : FMCSA has devoted a small but increasing amount of resources to develop the Compliance, Safety, Accountability program but is requesting a significant increase for full implementation / / [Susan Fleming]
	Pubbl/distr/stampa	Washington, DC : , : U.S. Govt. Accountability Office, , [2011]
	Descrizione fisica	1 online resource (8 pages) : illustrations
	Soggetti	Traffic safety - United States - Finance Trucks - State supervision - United States Buses - State supervision - United States
	Lingua di pubblicazione	Inglese
	Formato	Materiale a stampa
	Livello bibliografico	Monografia
	Note generali	Title from PDF title screen (viewed Sept. 12, 2011). "February 25, 2011." "GAO-11-416 R."
	Nota di bibliografia	Includes bibliographical references.