1. Record Nr. UNISA990003374270203316

Titolo	Assia Djebar / sous la direction de Najib Redouane, Yvette Bénayoun-Szmidt
Pubbl/distr/stampa	Paris : l'Harmattan, copyr. 2008
ISBN	978-2- 296-05194-2
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Collana	Autour des écrivains maghrébins
Disciplina	843
Soggetti	Djebar , Assia (1936-....) - Critica e interpretazione
Collocazione	II.10.B.40
Lingua di pubblicazione	Francese
Formato	Materiale a stampa
Livello bibliografico	Monografia

2. Record Nr. UNISA990006172990203316

Autore	LAFERRERE, Gregorio de
Titolo	Locos de verano / Gregorio de Laferrere
Pubbl/distr/stampa	[Buenos Aires] : Editorial Abril (, 1983)
Descrizione fisica	122 p. ; 20 cm
Collana	Coleccion Clasicos de la literatura argentina ; 11
Disciplina	863
Soggetti	Letteratura drammatica spagnola
Collocazione	VI.7.A. 39
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Pubbl/distr/stampa	San Francisco, Calif. : Morgan Kaufmann, 2005
ISBN	9780120884766 0120884763
Descrizione fisica	300 p.
Altri autori (Persone)	Franklin, Mark A., 1940-
Disciplina	621.395
Soggetti	Network processors - Design Application-specific integrated circuits - Design Electronic books.
Lingua di pubblicazione	Inglese
Formato	Risorsa elettronica
Livello bibliografico	Monografia
Nota di contenuto	1. Network Processors: New Horizons -- Patrick Crowley, Mark A. Franklin, Haldun Hadimioglu, Peter Z. Onufryk -- 2. Supporting Mixed Real-Time Workloads in -- Multithreaded Processors with Segmented -- Instruction Caches -- Patrick Crowley -- 3. Efficient Packet Classification with Digest Caches -- Francis Chang, Wu-chang Feng, Wu-chi Feng, Kang Li -- 4 Towards a Flexible Network Processor Interface for -- RapidIO, Hypertransport, and PCI-Express -- Christian Sauer, Matthias Gries, Kurt Keutzer, Jose Ignacio Gomez -- 5. A High-Speed, Multithreaded TCP Offload Engine for 10 Gb/s Ethernet -- Yatin Hoskote, Sriram Vangal, Vasantha Erraguntla, Nitin Borkar -- 6. A Hardware Platform for Network Intrusion Detection and Prevention -- Chris Clark,Wenke Lee, David Schimmel, Didier Contis, Mohamed Ko, Ashley Thomas -- 7. Packet Processing on a SIMD Stream Processor -- Jathin S. Rai, Yu-Kuen Lai, Gregory T. Byrd -- 8. A Programming Environment for Packet-Processing -- Systems: Design Considerations -- Harrick Vin, Jayaram Mudigonda, Jamie Jason, Erik J. Johnson,Roy Ju, Aaron Kunze, Ruiqi Lian -- 9. RNOSA Middleware Platform for Low-Cost -- Packet-Processing Devices -- Jonas Greutert, Lothar Thiele -- 10. On the Feasibility of Using Network Processors for DNA Queries -- Herbert Bos, Kaiming Huang -- 11. Pipeline Task Scheduling on Network Processors -- Mark A. Franklin, Seema Datar -- 12. A

Framework for Design Space Exploration of Resource Efficient Network Processing on Multiprocessor SoCs -- Matthias Grünewald, Jrg-Christian Niemann, Mario Porrmann, Ulrich Rückert -- 13. Application Analysis and Resource Mapping -- for Heterogeneous Network Processor Architectures -- Ramaswamy Ramaswamy, Ning Weng, Tilman Wolf -- References -- Index.

Sommario/riassunto

The past few years have seen significant change in the landscape of high-end network processing. In response to the formidable challenges facing this emerging field, the editors of this series set out to survey the latest research and practices in the design, programming, and use of network processors. Through chapters on hardware, software, performance and modeling, Volume 3 illustrates the potential for new NP applications, helping to lay a theoretical foundation for the architecture, evaluation, and programming of networking processors. Like Volume 2 of the series, Volume 3 further shifts the focus from achieving higher levels of packet processing performance to addressing other critical factors such as ease of programming, application developments, power, and performance prediction. In addition, Volume 3 emphasizes forward-looking, leading-edge research in the areas of architecture, tools and techniques, and applications such as high-speed intrusion detection and prevention system design, and the implementation of new interconnect standards. *Investigates current applications of network processor technology at Intel; Infineon Technologies; and NetModule. Presents current research in network processor design in three distinct areas: *Architecture at Washington University, St. Louis; Oregon Health and Science University; University of Georgia; and North Carolina State University. *Tools and Techniques at University of Texas, Austin; Academy of Sciences, China; University of Paderborn, Germany; and University of Massachusetts, Amherst. *Applications at University of California, Berkeley; Universidad Complutense de Madrid, Spain; ETH Zurich, Switzerland; Georgia Institute of Technology; Vrije Universiteit, the Netherlands; and Universiteit Leiden, the Netherlands.