

1. Record Nr.	UNISALENTO991000713749707536
Titolo	Guide to evaluation of the response of occupants of fixed structures, especially buildings and offshore structures, to low-frequency horizontal motion (0.063 Hz to 1 Hz) : BS 6611: 1985 / BSI
Pubbl/distr/stampa	London : British Standards Institution, c1999
ISBN	0580144925
Descrizione fisica	ii, 10 p. ; 28 cm
Collana	British Standard ; BS 6611: 1985
Altri autori (Enti)	British Standards Institution.Standards Policy Committee General Mechanical Engineering.Technical Committee GME/21
Disciplina	620.82
Soggetti	Human engineering - Standards Biomechanics - Standards
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Prepared by the General Mechanical Engineering Standards Policy Committee (GME/-) to Technical Committee GME/21
Nota di bibliografia	Includes bibliographical references

2. Record Nr.	UNINA9910485025903321
Titolo	Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation : 18th International Workshop, PATMOS 2008, Lisbon, Portugal, September 10-12, 2008, Revised Selected Papers // edited by Lars Svensson, José Monteiro
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2009
ISBN	3-540-95948-3
Edizione	[1st ed. 2009.]
Descrizione fisica	1 online resource (XIII, 462 p.)
Collana	Theoretical Computer Science and General Issues, , 2512-2029 ; ; 5349
Classificazione	DAT 190f ELT 272f SS 4800
Altri autori (Persone)	SvenssonLars <1960-> MonteiroJose <1966->
Disciplina	620/.004202825536
Soggetti	Logic design Microprocessors Computer architecture Electronic digital computers - Evaluation Computer arithmetic and logic units Computer storage devices Memory management (Computer science) Electronic circuits Logic Design Processor Architectures System Performance and Evaluation Arithmetic and Logic Structures Computer Memory Structure Electronic Circuits and Systems
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Session 1: Low-Leakage and Subthreshold Circuits -- Subthreshold FIR Filter Architecture for Ultra Low Power Applications -- Reverse Vgs

Static CMOS (RVGS-SCMOS); A New Technique for Dynamically Compensating the Process Variations in Sub-threshold Designs -- Improving the Power-Delay Performance in Subthreshold Source-Coupled Logic Circuits -- Design and Evaluation of Mixed 3T-4T FinFET Stacks for Leakage Reduction -- Session 2: Low-Power Methods and Models -- Temporal Discharge Current Driven Clustering for Improved Leakage Power Reduction in Row-Based Power-Gating -- Intelligate: Scalable Dynamic Invariant Learning for Power Reduction -- Analysis of Effects of Input Arrival Time Variations on On-Chip Bus Power Consumption -- Power-Aware Design via Micro-architectural Link to Implementation -- Untraditional Approach to Computer Energy Reduction -- Session 3: Arithmetic and Memories -- Mixed Radix-2 and High-Radix RNS Bases for Low-Power Multiplication -- Power Optimization of Parallel Multipliers in Systems with Variable Word-Length -- A Design Space Comparison of 6T and 8T SRAM Core-Cells -- Latched CMOS DRAM Sense Amplifier Yield Analysis and Optimization -- Session 4: Variability and Statistical Timing -- Understanding the Effect of Intradie Random Process Variations in Nanometer Domino Logic -- A Study on CMOS Time Uncertainty with Technology Scaling -- Static Timing Model Extraction for Combinational Circuits -- A New Bounding Technique for Handling Arbitrary Correlations in Path-Based SSTA -- Statistical Modeling and Analysis of Static Leakage and Dynamic Switching Power -- Session 5: Synchronization and Interconnect -- Logic Synthesis of Handshake Components Using Structural Clustering Techniques -- Fast Universal Synchronizers -- A Performance-Driven Multilevel Framework for the X-Based Full-Chip Router -- PMD: A Low-Power Code for Networks-on-Chip Based on Virtual Channels -- Session 6: Power Supplies and Switching Noise -- Near-Field Mapping System to Scan in Time Domain the Magnetic Emissions of Integrated Circuits -- A Comparison between Two Logic Synthesis Forms from Digital Switching Noise Viewpoint -- Generating Worst-Case Stimuli for Accurate Power Grid Analysis -- Monolithic Multi-mode DC-DC Converter with Gate Voltage Optimization -- Session 7: Low-Power Circuits; Reconfigurable Architectures -- Energy Efficiency of Power-Gating in Low-Power Clocked Storage Elements -- A New Dynamic Logic Circuit Design for an Effective Trade-Off between Noise-Immunity, Performance and Energy Dissipation -- Energy Efficient Elliptic Curve Processor -- Energy Efficient Coarse-Grain Reconfigurable Array for Accelerating Digital Signal Processing -- Power-Efficient Reconfiguration Control in Coarse-Grained Dynamically Reconfigurable Architectures -- Poster Session 1: Circuits and Methods -- Settling-Optimization-Based Design Approach for Three-Stage Nested-Miller Amplifiers -- Ultra Low Voltage High Speed Differential CMOS Inverter -- Differential Capacitance Analysis -- Automated Synchronous-to-Asynchronous Circuits Conversion: A Survey -- Novel Cross-Transition Elimination Technique Improving Delay and Power Consumption for On-Chip Buses -- Poster Session 2: Power and Delay Modeling -- Analytical High-Level Power Model for LUT-Based Components -- A Formal Approach for Estimating Embedded System Execution Time and Energy Consumption -- Power Dissipation Associated to Internal Effect Transitions in Static CMOS Gates -- Disjoint Region Partitioning for Probabilistic Switching Activity Estimation at Register Transfer Level -- Data Dependence of Delay Distribution for a Planar Bus -- Special Session: Power Optimizations Addressing Reconfigurable Architectures -- Towards Novel Approaches in Design Automation for FPGA Power Optimization -- Smart Enumeration: A Systematic Approach to Exhaustive Search -- An Efficient Approach for Managing Power Consumption Hotspots

Distribution on 3D FPGAs -- Interconnect Power Analysis for a Coarse-Grained Reconfigurable Array Processor -- Keynotes (Abstracts) -- Integration of Power Management Units onto the SoC -- Model to Hardware Matching for nm Scale Technologies -- Power and Profit: Engineering in the Envelope.

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Sommario/riassunto

This book constitutes the thoroughly refereed post-conference proceedings of 18th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2008, featuring Integrated Circuit and System Design, held in Lisbon, Portugal during September 10-12, 2008. The 31 revised full papers and 10 revised poster papers presented together with 3 invited talks and 4 papers from a special session on reconfigurable architectures were carefully reviewed and selected from numerous submissions. The papers are organized in topical sections on low-leakage and subthreshold circuits, low-power methods and models, arithmetic and memories, variability and statistical timing, synchronization and interconnect, power supplies and switching noise, low-power circuits; reconfigurable architectures, circuits and methods, power and delay modeling, as well as power optimizations addressing reconfigurable architectures.

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