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| 1. Record Nr. | UNISALENTO991000614249707536 |
| Autore | Conrad, Joseph |
| Titolo | Youth; Heart of darkness ; The end of the tether / Joseph Conrad |
| Pubbl/distr/stampa | London : Dent & sons, 1967 |
| Descrizione fisica | VIII, 344 p. ; 18 cm. |
| Collana | Collected edition of the works of Joseph Conrad |
| Disciplina | 823.912 |
| Lingua di pubblicazione | Inglese |
| Formato | Materiale a stampa |
| Livello bibliografico | Monografia |
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| 2. Record Nr. | UNINA9910830000903321 |
| Autore | Stocker Alan |
| Titolo | Analog VLSI circuits for the perception of visual motion [[electronic resource] /] / Alan Stocker |
| Pubbl/distr/stampa | Hoboken NJ, : John Wiley & Sons, 2006 |
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| Edizione | [1st edition] |
| Descrizione fisica | 1 online resource (243 p.) |
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| Disciplina | 006.37 |
| Soggetti | Computer vision
Motion perception (Vision) - Computer simulation
Neural networks (Computer science) |
| Lingua di pubblicazione | Inglese |
| Formato | Materiale a stampa |
| Livello bibliografico | Monografia |
| Note generali | Description based upon print version of record. |
| Nota di bibliografia | Includes bibliographical references and index. |
| Nota di contenuto | Analog VLSI Circuits for the Perception of Visual Motion; Contents; |

Foreword; Preface; 1 Introduction; 1.1 Artificial Autonomous Systems; 1.2 Neural Computation and Analog Integrated Circuits; 2 Visual Motion Perception; 2.1 Image Brightness; 2.2 Correspondence Problem; 2.3 Optical Flow; 2.4 Matching Models; 2.4.1 Explicit matching; 2.4.2 Implicit matching; 2.5 Flow Models; 2.5.1 Global motion; 2.5.2 Local motion; 2.5.3 Perceptual bias; 2.6 Outline for a Visual Motion Perception System; 2.7 Review of a VLSI Implementations; 3 Optimization Networks; 3.1 Associative Memory and Optimization 3.2 Constraint Satisfaction Problems 3.3 Winner-takes-all Networks; 3.3.1 Network architecture; 3.3.2 Global convergence and gain; 3.4 Resistive Network; 4 Visual Motion Perception Networks; 4.1 Model for Optical Flow Estimation; 4.1.1 Well-posed optimization problem; 4.1.2 Mechanical equivalent; 4.1.3 Smoothness and sparse data; 4.1.4 Probabilistic formulation; 4.2 Network Architecture; 4.2.1 Non-stationary optimization; 4.2.2 Network conductances; 4.3 Simulation Results for Natural Image Sequences; 4.4 Passive Non-linear Network Conductances; 4.5 Extended Recurrent Network Architectures 4.5.1 Motion segmentation 4.5.2 Attention and motion selection; 4.6 Remarks; 5 Analog VLSI Implementation; 5.1 Implementation Substrate; 5.2 Phototransduction; 5.2.1 Logarithmic adaptive photoreceptor; 5.2.2 Robust brightness constancy constraint; 5.3 Extraction of the Spatio-temporal Brightness Gradients; 5.3.1 Temporal derivative circuits; 5.3.2 Spatial sampling; 5.4 Single Optical Flow Unit; 5.4.1 Wide-linear-range multiplier; 5.4.2 Effective bias conductance; 5.4.3 Implementation of the smoothness constraint; 5.5 Layout; 6 Smooth Optical Flow Chip; 6.1 Response Characteristics 6.1.1 Speed tuning 6.1.2 Contrast dependence; 6.1.3 Spatial frequency tuning; 6.1.4 Orientation tuning; 6.2 Intersection-of-constraints Solution; 6.3 Flow Field Estimation; 6.4 Device Mismatch; 6.4.1 Gradient offsets; 6.4.2 Variations across the array; 6.5 Processing Speed; 6.6 Applications; 6.6.1 Sensor modules for robotic applications; 6.6.2 Human-machine interface; 7 Extended Network Implementations; 7.1 Motion Segmentation Chip; 7.1.1 Schematics of the motion segmentation pixel; 7.1.2 Experiments and results; 7.2 Motion Selection Chip; 7.2.1 Pixel schematics 7.2.2 Non-linear diffusion length 7.2.3 Experiments and results; 8 Comparison to Human Motion Vision; 8.1 Human vs. Chip Perception; 8.1.1 Contrast-dependent speed perception; 8.1.2 Bias on perceived direction of motion; 8.1.3 Perceptual dynamics; 8.2 Computational Architecture; 8.3 Remarks; Appendix; A Variational Calculus; B Simulation Methods; C Transistors and Basic Circuits; D Process Parameters and Chips Specifications; References; Index

Sommario/riassunto

Although it is now possible to integrate many millions of transistors on a single chip, traditional digital circuit technology is now reaching its limits, facing problems of cost and technical efficiency when scaled down to ever-smaller feature sizes. The analysis of biological neural systems, especially for visual processing, has allowed engineers to better understand how complex networks can effectively process large amounts of information, whilst dealing with difficult computational challenges. Analog and parallel processing are key characteristics of biological neural networks. Analog VL