1. Record Nr. UNINA990002603730403321

| | |
|---|---|
| Autore | Dickinson, John P. |
| Titolo | Portfolio analysis / di DICKINSON J. |
| Pubbl/distr/stampa | Westmead : Saxon House, 1974 |
| Locazione | ECA<br>DECTS |
| Collocazione | 5-1-23-TI<br>G1.29 |
| Lingua di pubblicazione | Inglese |
| Formato | Materiale a stampa |
| Livello bibliografico | Monografia |

2. Record Nr. UNINA9910312137303321

| | |
|---|---|
| Titolo | Gauguin : Galeries nationales du Grand Palais, Paris, 10 janvier-24 avril 1989 |
| Pubbl/distr/stampa | Paris : Éditions de la Reunion des museés nationaux, 1989 |
| ISBN | 2711822206 |
| Descrizione fisica | 494 p. : ill. ; 31 cm |
| Disciplina | 759.4 |
| Locazione | FARBC |
| Collocazione | ART.FI C 313 |
| Lingua di pubblicazione | Francese |
| Formato | Materiale a stampa |
| Livello bibliografico | Monografia |
| Note generali | Sul frontespizio: Ministère da la culture, de la communication, des grands travaux et du bicentenaire<br>Catalogo della mostra |

3. Record Nr. UNINA9910422955803321

| | |
|---|---|
| Autore | Maslin, Mark |
| Titolo | Riscaldamento globale / Mark Maslin ; traduzione di Giuliano Olivero |
| Pubbl/distr/stampa | Torino, : Codice, 2007 |
| ISBN | 978-88-7578-081-4 |
| Descrizione fisica | XI, 185 p. : ill. ; 18 cm |
| Collana | Codice paperback |
| Disciplina | 363.73874 |
| Locazione | FAGBC |
| Collocazione | 60 363.738 MASM 2007 |
| Lingua di pubblicazione | Italiano |
| Formato | Materiale a stampa |
| Livello bibliografico | Monografia |

4. Record Nr. UNISALENTO991000538269707536

| | |
|---|---|
| Autore | Aristoteles |
| Titolo | Sull'educazione / a cura di George Howie e Piero Innocenti |
| Pubbl/distr/stampa | Firenze : La nuova Italia, 1973 |
| Descrizione fisica | 260 p. ; 21 cm |
| Collana | Educatori antichi e moderni ; 268 |
| Altri autori (Persone) | Howie, George<br>Innocenti, Piero |
| Disciplina | 370.1 |
| Lingua di pubblicazione | Italiano |
| Formato | Materiale a stampa |
| Livello bibliografico | Monografia |

5. Record Nr. UNISALENTO991001360819707536

| | |
|---|---|
| Autore | Cavalera, Francesco |
| Titolo | Spazi di lunghezza. Tesi di laurea / laureando Francesco Cavalera ; relat. G. De Cecco |
| Pubbl/distr/stampa | Lecce : Università degli studi. Facoltà di Scienze. Corso di laurea in Matematica, a.a. 1986-87 |
| Classificazione | AMS 51K05 |
| Altri autori (Persone) | De Cecco, Giuseppe |
| Disciplina | 516.37 |
| Soggetti | General theory |
| Lingua di pubblicazione | Italiano |
| Formato | Materiale a stampa |
| Livello bibliografico | Monografia |

6. Record Nr. UNINA9910830214603321

| | |
|---|---|
| Autore | Staszewski Robert Bogdan <1965-> |
| Titolo | All-digital frequency synthesizer in deep-submicron CMOS [[electronic resource] /] / Robert Bogdan Staszewski, Poras T. Balasara |
| Pubbl/distr/stampa | Hoboken, N.J., : Wiley-Interscience, c2006 |
| ISBN | 1-280-65439-2<br>9786610654390<br>0-470-04195-1<br>0-470-04194-3 |
| Edizione | [1st edition] |
| Descrizione fisica | 1 online resource (281 p.) |
| Altri autori (Persone) | BalsaraPoras T. <1961-> |
| Disciplina | 621.3815363<br>621.3815486 |
| Soggetti | Frequency synthesizers - Design and construction<br>Wireless communication systems - Equipment and supplies - Design and construction<br>Metal oxide semiconductors, Complementary - Design and construction |
| Lingua di pubblicazione | Inglese |
| Formato | Materiale a stampa |

| | |
|---|---|
| Livello bibliografico | Monografia |
| Note generali | Description based upon print version of record. |
| Nota di bibliografia | Includes bibliographical references (p. 247-252) and index. |
| Nota di contenuto | ALL-DIGITAL FREQUENCY SYNTHESIZER IN DEEP-SUBMICRON CMOS; CONTENTS; PREFACE; Acknowledgments; 1 INTRODUCTION; 1.1 Frequency Synthesis; 1.1.1 Noise in Oscillators; 1.1.2 Frequency Synthesis Techniques; 1.2 Frequency Synthesizer as an Integral Part of an RF Transceiver; 1.2.1 Transmitter; 1.2.2 Receiver; 1.2.3 Toward Direct Transmitter Modulation; 1.3 Frequency Synthesizers for Mobile Communications; 1.3.1 Integer-N PLL Architecture; 1.3.2 Fractional-N PLL Architecture; 1.3.3 Toward an All-Digital PLL Approach; 1.4 Implementation of an RF Synthesizer<br>1.4.1 CMOS vs. Traditional RF Process Technologies1.4.2 Deep-Submicron CMOS; 1.4.3 Digitally Intensive Approach; 1.4.4 System Integration; 1.4.5 System Integration Challenges for Deep-Submicron CMOS; 2 DIGITALLY CONTROLLED OSCILLATOR; 2.1 Varactor in a Deep-Submicron CMOS Process; 2.2 Fully Digital Control of Oscillating Frequency; 2.3 LC Tank; 2.4 Oscillator Core; 2.5 Open-Loop Narrowband Digital-to-Frequency Conversion; 2.6 Example Implementation; 2.7 Time-Domain Mathematical Model of a DCO; 2.8 Summary; 3 NORMALIZED DCO; 3.1 Oscillator Transfer Function and Gain; 3.2 DCO Gain Estimation<br>3.3 DCO Gain Normalization3.4 Principle of Synchronously Optimal DCO Tuning Word Retiming; 3.5 Time Dithering of DCO Tuning Input; 3.5.1 Oscillator Tune Time Dithering Principle; 3.5.2 Direct Time Dithering of Tuning Input; 3.5.3 Update Clock Dithering Scheme; 3.6 Implementation of PVT and Acquisition DCO Bits; 3.7 Implementation of Tracking DCO Bits; 3.7.1 High-Speed Dithering of Fractional Varactors; 3.7.2 Dynamic Element Matching of Varactors; 3.7.3 DCO Varactor Rearrangement; 3.8 Time-Domain Model; 3.9 Summary; 4 ALL-DIGITAL PHASE-LOCKED LOOP; 4.1 Phase-Domain Operation<br>4.2 Reference Clock Retiming4.3 Phase Detection; 4.3.1 Difference Mode of ADPLL Operation; 4.3.2 Integer-Domain Operation; 4.4 Modulo Arithmetic of the Reference and Variable Phases; 4.4.1 Variable-Phase Accumulator (PV Block); 4.5 Time-to-Digital Converter; 4.5.1 Frequency Reference Edge Estimation; 4.6 Fractional Error Estimator; 4.6.1 Fractional-Division Ratio Compensation; 4.6.2 TDC Resolution Effect on Estimated Frequency Resolution; 4.6.3 Active Removal of Fractional Spurs Through TDC (Optional); 4.7 Frequency Reference Retiming by a DCO Clock; 4.7.1 Sense Amplifier-Based Flip-Flop<br>4.7.2 General Idea of Clock Retiming4.7.3 Implementation; 4.7.4 Time-Deferred Calculation of the Variable Phase (Optional); 4.8 Loop Gain Factor; 4.8.1 Phase-Error Dynamic Range; 4.9 Phase-Domain ADPLL Architecture; 4.9.1 Close-in Spurs Due to Injection Pulling; 4.10 PLL Frequency Response; 4.10.1 Conversion Between the s- and z-Domains; 4.11 Noise and Error Sources; 4.11.1 TDC Resolution Effect on Phase Noise; 4.11.2 Phase Noise Due to DCO Dithering; 4.12 Type II ADPLL; 4.12.1 PLL Frequency Response of a Type II Loop; 4.13 Higher-Order ADPLL; 4.13.1 PLL Stability Analysis<br>4.14 Nonlinear Differential Term of an ADPLL |
| Sommario/riassunto | A new and innovative paradigm for RF frequency synthesis and wireless transmitter design Learn the techniques for designing and implementing an all-digital RF frequency synthesizer. In contrast to traditional RF techniques, this innovative book sets forth digitally intensive design techniques that lead the way to the development of low-cost, low-power, and highly integrated circuits for RF functions in |

deep submicron CMOS processes. Furthermore, the authors demonstrate how the architecture enables readers to integrate an RF front-end with the digital back-end onto a single silicon die