

1. Record Nr.	UNISALENTO991000243259707536
Autore	Chu, Wai C., 1967-
Titolo	Speech coding algorithms : foundation and evolution of standardized coders / Wai C. Chu
Pubbl/distr/stampa	Hoboken, N.J. : J. Wiley & Sons, 2003
ISBN	0471373125
Descrizione fisica	xxiv, 558 p. : ill. ; 24 cm
Disciplina	621.3822
Soggetti	Speech processing systems Coding theory Algorithms
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	"A Wiley-Interscience publication."
Nota di bibliografia	Includes bibliographical references and index

2. Record Nr.	UNINA9910820686903321
Autore	Xiu Liming
Titolo	Nanometer frequency synthesis beyond the phase-locked loop // Liming Xiu
Pubbl/distr/stampa	Hoboken [New Jersey] : , : John Wiley & Sons, , 2012 [Piscataway, New Jersey] : , : IEEE Xplore, , [2012]
ISBN	1-280-79376-7 9786613704153 1-118-34794-3 1-118-34795-1 1-118-34792-7
Descrizione fisica	1 online resource (340 p.)
Collana	IEEE Press Series on Microelectronic Systems ; ; v.25
Disciplina	621.381/32
Soggetti	Timing circuits Frequency synthesizers Very high speed integrated circuits
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	PREFACE xi -- 1 CLOCK SIGNAL IN ELECTRONIC SYSTEMS 1 -- 1.1 The Significance of Clock Signal 1 -- 1.2 The Characteristics of Clock Signal 5 -- 1.3 Clock Signal Driving Digital System 18 -- 1.4 Clock Signal Driving Sampling System 24 -- 1.5 Extracting Clock Signal From Data: Clock Data Recovery 30 -- 1.6 Clock Usage in System-on-Chip 32 -- 1.7 Two Fields: Clock Generation and Clock Distribution 33 -- 2 CLOCK GENERATION: EXISTING FREQUENCY SYNTHESIS TECHNIQUES 37 -- 2.1 Direct Analog Frequency Synthesis 38 -- 2.2 Direct Digital Frequency Synthesis 39 -- 2.3 Indirect Method (Phase-Locked Loop Based) 41 -- 2.4 The Shared Goal: All Cycles Have Same Length-in-Time 51 -- 3 TIME-AVERAGE-FREQUENCY 53 -- 3.1 The Scale of Level and the Scale of Time 53 -- 3.2 What Is Frequency? 54 -- 3.3 Reinvestigating the Frequency Concept: the Birth of Time-Average-Frequency 56 -- 3.4 Time-Average-Frequency in Circuit Implementation 59 -- 3.5 Average Frequency, Time-Average-Frequency, and Fundamental Frequency 61 -- 3.6 The Need of a Theory 62 -- 3.7 The Summary: Why Do We Need

Time-Average-Frequency?	63
4 FLYING-ADDER DIRECT PERIOD SYNTHESIS ARCHITECTURE	65
4.1 The Working Principle	65
4.2 The Major Challenges in the Flying-Adder Circuit	68
4.3 The Circuit of Proof of Concept	74
4.4 The Working Circuitry	77
4.5 Frequency Transfer Function, Frequency Range, Frequency Resolution, and Frequency Switching Speed	87
4.6 The Technique of Post Divider Fractional Bits Recovery	88
4.7 Flying-Adder PLL: FAPLL	90
4.8 Flying-Adder Fractional Divider	91
4.9 Integer-Flying-Adder Architecture	92
4.10 The Algorithm to Search Optimum Parameters	98
4.11 The Construction of the Accumulator	99
4.12 The Construction of the High Speed Multiplex	104
4.13 Non-2's Power Flying-Adder Circuit	107
4.14 Expanding VCO Frequency Range in Nanometer CMOS Processes	109
4.15 Multiple Flying-Adder Synthesizers	110
4.16 Flying-Adder Implementation Styles	111
4.17 Simulation Approaches	112
4.18 The Impact of Input Mismatch on Output Jitter	113
4.19 Flying-Adder Circuit as Digital Controlled Oscillator	127
4.20 Flying-Adder Terminology	128
4.21 Flying-Adder Synthesizer and Time-Average-Frequency: The Experimental Evidence	129
4.22 Time-Average-Frequency and Setup Constraint: Revisit	154
4.23 Sense the Frequency Difference: The Time-Average-Frequency Way	156
4.24 Flying-Adder and Direct Digital Synthesis (DDS): The Difference	157
4.25 Flying-Adder for Phase (Delay) Synthesis	158
4.26 Flying-Adder for Duty Cycle Control	162
4.27 Flying-Adder Synthesizer in Reducing the Number of PLLs in SoC	163
5 DIGITAL-TO-FREQUENCY CONVERTER	167
5.1 Two Ways of Representing Information	167
5.2 The Converters for Transforming Information	168
5.3 The Two Cornerstones of the Digital-to-Frequency Converter	170
5.4 The Theoretical Foundation of Flying-Adder Digital-to-Frequency Converter	172
5.5 Convert the Spurious Energy to Noise Energy	193
5.6 Move Spurs Around	198
5.7 Spread the Energy	201
5.8 Performance Merits	205
6 THE NEW FRONTIER IN ELECTRONIC SYSTEM DESIGN	211
6.1 The Clocking Challenges in Reality	211
6.2 Flying-Adder and Its Three Major Application Areas	216
6.3 Flying-Adder for On-chip Frequency Generation	218
6.4 Flying-Adder as Adaptive Clock Generator	222
6.5 Flying-Adder as On-chip VCXO	230
6.6 Flying-Adder for Frame Rate Synchronization and Display Monitor Accommodation	237
6.7 Flying-Adder for Frequency Synchronization in Digital Communication: A Preview	240
6.8 Flying-Adder for Clock Data Recovery	242
6.9 Flying-Adder DLL for Deskew	255
6.10 Flying-Adder for Digital Frequency-Locked Loop (Flying-Adder DFLL)	256
6.11 Flying-Adder for Digital Phase-Locked Loop (Flying-Adder DPLL)	262
6.12 Flying-Adder Technology for Dynamic Frequency Scaling	262
6.13 Flying-Adder as 1-bit DDFS	264
6.14 Flying-Adder for Spread Spectrum Clocking	265
6.15 Flying-Adder for Driving Sampling System	268
6.16 Flying-Adder for Non-uniform Sampling	271
6.17 Flying-Adder as Digital FSK Modulator	273
6.18 Flying-Adder for PWM/PFW DC-DC Power Conversion	274
6.19 Integrate Clocking Chips into Processing Chips	275
7 LOOKING INTO FUTURE: THE ERA OF "TIME"	279
7.1 The Four Fundamental Technologies in Modern Chip Design	279
7.2 "Time"-Based Analog Processing	281
7.3 "Time" and Frequency: Encoding Messages Through Modulation	283
7.4 Manipulate "Time": The Tools	283
7.5 It Is Time to Use "Time"	284
APPENDICES	287
Appendix 4.A: The VHDL Code for Flying-Adder Synthesizer	287
Appendix 4.B: How Close Can It Reach an Integer?	296
Appendix 4.C: The Seed and Set in Integer-Flying-Adder PLL	299
Appendix 4.D: The Number of Carries From an XIU-	

Accumulator 302 -- Appendix 5.A: The Flying-Adder State Machine Model (perl) 303 -- Appendix 5.B: The Flying-Adder Waveform Generator (perl) 307 -- Appendix 5.C: The Flying-Adder Waveform Generator with Triangular Modulation (perl) 310 -- Appendix 5.D: The Flying-Adder Waveform Generator with Random Modulation (perl) 314 -- Appendix 6.A: The FA-DCXO Tangent Line and Linearity Measurement 318.
INDEX 321.

Sommario/riassunto

Introducing a new, pioneering approach to integrated circuit design, *Nanometer Frequency Synthesis Beyond Phase-Locked Loop* introduces an innovative new way of looking at frequency that promises to open new frontiers in modern integrated circuit (IC) design. While most books on frequency synthesis deal with the phase-locked loop (PLL), this book focuses on the clock signal. It revisits the concept of frequency, solves longstanding problems in on-chip clock generation, and presents a new time-based information processing approach for future chip design. Beginning with the basics, the book explains how clock signal is used in electronic applications and outlines the shortcomings of conventional frequency synthesis techniques for dealing with clock generation problems. It introduces the breakthrough concept of Time-Average-Frequency, presents the Flying-Adder circuit architecture for the implementation of this approach, and reveals a new circuit device, the Digital-to-Frequency Converter (DFC). Lastly, it builds upon these three key components to explain the use of time rather than level to represent information in signal processing. Provocative, inspiring, and chock-full of ideas for future innovations, the book features: . A new way of thinking about the fundamental concept of clock frequency. A new circuit architecture for frequency synthesis: the Flying-Adder direct period synthesis. A new electronic component: the Digital-to-Frequency Converter. A new information processing approach: time-based vs. level-based. Examples demonstrating the power of this technology to build better, cheaper, and faster systems. Written with the intent of showing readers how to think outside the box, *Nanometer Frequency Synthesis Beyond the Phase-Locked Loop* is a must-have resource for IC design engineers and researchers as well as anyone who would like to be at the forefront of modern circuit design.
