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Nota di contenuto	First Twenty Years of the International Symposium on Applied Reconfigurable Computing (ARC): a Selection of Papers -- HT-NoC: Reconfigurable High Throughput Network-on-Chip for AI Dataflow Accelerators -- An MLIR-based Compilation Framework for CGRA Application Deployment -- Hardware-Accelerated Event-Graph Neural Networks for Low-Latency Time-Series Classification on SoC FPGA -- RePAIR: Reconfigurable Platform for AI Resilience within RISC-V Ecosystem -- ROBoost: A Study of FPGA Logic-Based Power-Wasting Primitives -- FLARE: An FPGA-based Universal Large Flow Detection Engine -- Out-of-the-Box Performance of FPGAs for ML Workloads using Vitis AI -- A Heterogeneous Embedded Platform for AI-based Protocol Identification -- Counting Heavy Items in Filtered Data Streams Using an HLS-Generated FPGA Kernel -- Ultra-low Latency and Extreme Throughput Echo State Neural Networks on FPGA -- A Reconfigurable Stream-Based FPGA Accelerator for Bayesian Confidence

Propagation Neural Networks -- Real-Time Multi-Object Tracking using YOLOv8 and SORT on a SoC FPGA -- Dynamic Function Exchange in FPGA to Redefine RISC-V Multicore Architectures at Runtime.

Sommario/riassunto

This book constitutes the proceedings of the 21st International Symposium on Applied Reconfigurable Computing. Architectures, Tools, and Applications, ARC 2025, held in Seville, Spain, during April 9–11, 2025. The 12 full papers presented in this book together with 1 short paper from the technical program were carefully reviewed and selected from 40 submissions. ARC 2025 covers a wide range of topics, including hardware acceleration, security and fault tolerance, energy-efficient architectures, and emerging applications in artificial intelligence and high-performance computing. The symposium fostered collaboration and pushed the boundaries of state-of-the-art research.
