

1. Record Nr.	UNISA996647868203316
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Titolo	Algorithms and Architectures for Parallel Processing : 24th International Conference, ICA3PP 2024, Macau, China, October 29–31, 2024, Proceedings, Part IV // edited by Tianqing Zhu, Jin Li, Aniello Castiglione
Pubbl/distr/stampa	Singapore : , : Springer Nature Singapore : , : Imprint : Springer, , 2025
ISBN	9789819615452 9819615453
Edizione	[1st ed. 2025.]
Descrizione fisica	1 online resource (492 pages)
Collana	Lecture Notes in Computer Science, , 1611-3349 ; ; 15254
Altri autori (Persone)	LiJin CastiglioneAniello
Disciplina	004.35
Soggetti	Algorithms Machine learning Computer engineering Computer networks Computer vision Design and Analysis of Algorithms Machine Learning Computer Engineering and Networks Computer Vision
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di contenuto	SMP-NoC: A Flexible and Efficient Shared Memory Protection Unit on Network-on-Chip -- A Fine-Grained Ownership Transfer Protocol for Cloud EMRs Auditing -- MARO: Enabling Full MPI Automatic Refactoring in DSL-based Programming Framework -- SSC: An SRAM-based Silence Computing Design for On-chip Memory -- TP-BFT: A Faster Asynchronous BFT Consensus with Parallel Structure -- LTP: A Lightweight On-chip Temporary Prefetcher for Data-dependent Memory Accesses -- A Neural Network-Based PUF Protection Method Against Machine Learning Attack -- Compression Format and Systolic Array Structure Co-design for Accelerating Sparse Matrix Multiplication

in DNNs -- Multidimensional Intrinsic Identity Construction and Dynamic Seamless Authentication Schemes in IoT Environments -- Invisible Backdoor Attack with Image Contours Triggers -- Finestra: Multi-Aggregator Swarm Learning for Gradient Leakage Defense -- DisFU: Protecting Innocent Clients in Federated Unlearning -- Multiple-Round Aggregation of Abstract Semantics for Secure Heterogeneous Federated Learning -- Dynamic Privacy Protection with Large Language Model in Social Networks -- A Dynamic Symmetric Searchable Encryption Scheme for Rapid Conjunctive Queries -- A Data Watermark Scheme base on Data Converted Bitmap for Data Trading -- Distributed Incentive Algorithm for Fine-grained Offloading in Vehicular Ad Hoc Networks -- Mitigating Over-Unlearning in Machine Unlearning with Synthetic Data Augmentation -- AW-YOLOv9: Adverse Weather Conditions Adaptation for UAV Detection.-Efficient and Privacy-preserving Ranking-based Federated Learning -- On-Chain Dynamic Policy Evaluation for Decentralized Access Control -- DPG-FairFL: A Dual-Phase GAN-based Defense Framework Against Image-based Fairness Data Poisoning Attacks in Federated Learning.

Sommario/riassunto

The six-volume set, LNCS 15251-15256, constitutes the refereed proceedings of the 24th International Conference on Algorithms and Architectures for Parallel Processing, ICA3PP 2024, held in Macau, China, during October 29–31, 2024. The 91 full papers, 35 short papers and 5 workshop papers included in these proceedings were carefully reviewed and selected from 265 submissions. They focus on the many dimensions of parallel algorithms and architectures, encompassing fundamental theoretical approaches, practical experimental projects, and commercial components and systems.
