1. Record Nr. UNISA996559965803316

Titolo	62530-2-2023 - IEEE/IEC International Standard--SystemVerilog Part 2 : Universal Verification Methodology Language Reference Manual / / IEEE
Pubbl/distr/stampa	New York, USA : , : IEEE, , 2023
ISBN	979-88-557-0213-2
Descrizione fisica	1 online resource (461 pages)
Disciplina	160
Soggetti	Verification (Logic)
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Sommario/riassunto	The Universal Verification Methodology (UVM) that can improve interoperability, reduce the cost of using intellectual property (IP) for new projects or electronic design automation (EDA) tools, and make it easier to reuse verification components is provided. Overall, using this standard will lower verification costs and improve design quality throughout the industry. The primary audiences for this standard are the implementors of the UVM base class library, the implementors of tools supporting the UVM base class library, and the users of the UVM base class library.