1. Record Nr. UNINA9910481532203321

Autore	Brucioli Antonio <1487-1566.>
Titolo	La Biblia quale contiene i sacri libri del Vecchio Testamento, tradotti da la hebraica uerita in lingua toscana per Antonio Brucioli, aggiuntiui duoi libri di Esdra, & più capitoli in Daniel, & in Ester, nuouamente trouati, & il terzo libro de Machabei. Co diuini libri del Nuouo Testamento di Christo Giesu signore, & saluatore nostro. Tradotti dal greco pel medesimo. Con due tauole ... Con le concordantie del Nuouo & Vecchio Testamento [[electronic resource]]
Pubbl/distr/stampa	Venice, : Federico Torresano, d. 1561 or 62, 1539
Descrizione fisica	Online resource (2 v. ([4], 459, [1]; [4], 116 c.), 4°)
Altri autori (Persone)	NenciniGiovanni <1803-1878.> TorresanoFederico <1561 or 1562.> ZanettiBartholomeo <1486 or 1487.>
Lingua di pubblicazione	Italiano
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Reproduction of original in Biblioteca Nazionale Centrale di Firenze.

2. Record Nr. UNISA996550556703316

Titolo	Applied Reconfigurable Computing. Architectures, Tools, and Applications : 19th International Symposium, ARC 2023, Cottbus, Germany, September 27-29, 2023, Proceedings / / Francesca Palumbo [and three others], editors
Pubbl/distr/stampa	Cham, Switzerland : , : Springer Nature Switzerland AG, , [2023] ©2023
ISBN	3-031-42921-4
Edizione	[First edition.]
Descrizione fisica	1 online resource (380 pages)
Collana	Lecture Notes in Computer Science Series ; ; Volume 14251
Disciplina	004
Soggetti	Adaptive computing systems
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Intro -- Preface -- Organization -- Contents -- Design Methods and Tools -- High-Level Synthesis of Memory Systems for Decoupled Data Orchestration -- 1 Introduction -- 2 Background and Related Work -- 2.1 Taxonomy of Data Orchestration -- 2.2 Storage Idioms -- 3 PIPO: An Data Structure for Decoupled Data Orchestration -- 3.1 Definition of PIPO -- 3.2 Automatic Insertion of API Calls -- 4 Automatic Decoupling of Data Orchestration -- 4.1 RAM-Wise Decoupling -- 4.2 Decoupling Algorithm -- 4.3 Compilation Example -- 5 Automatic Partial Decoupling -- 5.1 Partial Decoupling Based on the Fork-Join Model -- 5.2 Automatically Determining the Fork and Join Points -- 6 BuffetLike: Another Data Structure for Decoupled Data Orchestration -- 7 Evaluation -- 7.1 Experimental Setup -- 7.2 Execution Time -- 7.3 Resource Utilization -- 7.4 Discussion -- 8 Conclusion -- References -- Rapid Prototyping of Complex Micro-architectures Through High-Level Synthesis -- 1 Introduction -- 2 Background and Motivation -- 2.1 Different Micro-architecture Design Tools -- 2.2 HLS Limitation in Pipelining an Instruction Set Simulator -- 3 Related Work -- 3.1 Deploying Speculative and Dynamic Techniques in HLS -- 3.2 Pipelined CPU Designs Using HLS -- 3.3 Dynamic Hart Scheduling in Multi-threaded CPU and GPU -- 4 Proposed Approach -- 4.1 Static Multi-threaded RISC-V Core -- 4.2 Dynamic Single-Threaded

RISC-V Core -- 4.3 Dynamic Multi-threaded RISC-V Core -- 4.4 Thread Synchronization -- 4.5 Shared-Memory RISC-V Multi-core -- 5 Experimental Validation -- 6 Conclusion -- References -- NVMulator: A Configurable Open-Source Non-volatile Memory Emulator for FPGAs -- 1 Introduction -- 2 Storage Technologies and Related Work -- 2.1 NVM Storage Technologies -- 2.2 Related Work -- 3 Proposed Approach -- 3.1 NVMulator Micro-Architecture -- 3.2 TaPaSCo Integration.
4 Experimental Setup and Evaluation -- 4.1 Latency -- 4.2 FIO Bandwidth -- 4.3 Database Application -- 5 Conclusion -- References -- On the OpenCL Support for Streaming Fixed-Function Accelerators on Embedded SoC FPGAs -- 1 Introduction -- 2 Related Work -- 3 Methodology -- 3.1 Application Software -- 3.2 Custom Device Driver and Kernel Interaction -- 4 CNN Application -- 5 Results and Discussion -- 6 Conclusion and Future Work -- References -- Design Space Exploration of Application Specific Number Formats Targeting an FPGA Implementation of SPICE -- 1 Introduction -- 2 Background -- 2.1 Related Work -- 2.2 Posit Numbers -- 2.3 Principle of Circuit Simulation with SPICE -- 3 Analysis of Number Formats in SPICE -- 3.1 Distribution of Operations -- 3.2 Impact on Convergence and Output Error -- 3.3 Impact on Simulation Runtime -- 4 Operator Implementation -- 5 Whole Application Analysis -- 6 Conclusion -- References -- Memory-Aware Scheduling for a Resource-Elastic FPGA Operating System -- 1 Introduction -- 2 Background and Related Work -- 2.1 DRAM Performance -- 2.2 Related Work -- 3 The Proposed Approach -- 3.1 Task's Memory Characteristics -- 3.2 Memory Model-Aware (MMA) Scheduling -- 3.3 Memory Access Pattern-Aware (MAPA) Scheduling -- 4 Evaluation -- 4.1 Evaluation Design -- 4.2 Results and Discussion -- 5 Conclusion -- References -- ArcvaVX: OpenVX Framework for Adaptive Reconfigurable Computer Vision Architectures -- 1 Introduction -- 2 Related Work -- 3 Framework -- 3.1 Library Module -- 3.2 Graph Creation Module -- 3.3 Hardware Creation Module -- 4 Evaluation -- 5 Conclusion -- References -- Applications -- FPGA-Integrated Bag of Little Bootstraps Accelerator for Approximate Database Query Processing -- 1 Introduction -- 2 Related Work -- 3 Architecture and Optimizations -- 3.1 Bag of Little Bootstraps for AQP -- 3.2 Streaming BLB.
3.3 Gauss Random Number Generator (GRNG) -- 3.4 BLB Block Design -- 4 Test Setup for Evaluation -- 4.1 Hardware Platform -- 4.2 Test System Structure -- 4.3 CPU Implementation -- 5 Evaluation -- 6 Conclusion -- References -- Accelerating Graph Neural Networks in Pytorch with HLS and Deep Dataflows -- 1 Introduction -- 2 Related Work and Motivation -- 3 Dataflow Description -- 3.1 Combination Engine -- 3.2 Aggregation Engine -- 4 Dataflow Optimization -- 5 Multi-threaded Extension -- 6 Pytorch Integration -- 7 Performance Evaluation -- 8 Conclusions -- References -- DNN Model Theft Through Trojan Side-Channel on Edge FPGA Accelerator -- 1 Introduction -- 2 Background -- 2.1 Versatile Tensor Accelerator -- 2.2 Reverse Engineering DNN Architecture -- 2.3 Threat Model -- 3 Methodology -- 3.1 Hardware Trojan Design -- 3.2 Predicting the Layer Hyperparameters -- 4 Experiment Results -- 4.1 Demonstration of Our Attack on ResNet18 -- 4.2 Evaluation of Our Attack on Randomly-chained DNNs -- 4.3 Hardware Trojan Overheads -- 5 Limitations and Future Work -- 6 Conclusion -- References -- Towards Secure and Efficient Multi-generation Cellular Communications: Multi-mode SNOW-3G/V ASIC and FPGA Implementations -- 1 Introduction -- 2 SNOW 3G and SNOW-V -- 2.1 The SNOW 3G Algorithm -- 2.2 The SNOW-V Algorithm -- 3 Proposed Multi-mode Architectures -- 3.1 SNOW-3G/V for Area Efficiency -- 3.2 SNOW-3G/V for High

Performance -- 4 Experimental Results and Comparisons -- 5 Conclusions -- References -- A Convolution Neural Network Based Displaced Vertex Trigger for the Belle II Experiment*-1pc -- 1 Introduction -- 2 State of the Art -- 3 Concept of a Displaced Vertex Trigger -- 3.1 Hit Image Converter -- 3.2 Parallel Convolution Layer -- 3.3 Training -- 3.4 Hardware Generator -- 4 Result -- 5 Summary -- References.
On-FPGA Spiking Neural Networks for Multi-variable End-to-End Neural Decoding -- 1 Introduction -- 2 Related Works -- 3 Methods -- 3.1 Neural Recording and Decoding Problem -- 3.2 Signal Processing: Spike Detection -- 3.3 Neural Decoding -- 3.4 Training Scheme -- 4 Hardware Architecture -- 4.1 PC-FPGA Communication -- 4.2 Spiking Neural Network Architecture -- 5 Discussion -- 5.1 Accuracy -- 5.2 Resource Utilization -- 5.3 Power Consumption -- 5.4 Adaptability to Different Experiments -- 6 Comparison with State of Art -- 7 Conclusion -- References -- Implementation of a Perception System for Autonomous Vehicles Using a Detection-Segmentation Network in SoC FPGA -- 1 Introduction -- 2 Previous Work -- 3 Implementation of the Perception and Control System -- 3.1 Detection-Segmentation Network in SoC FPGA -- 3.2 Vehicle Control Algorithm -- 3.3 Hardware Setup -- 4 Evaluation of the Detection-Segmentation Network -- 5 Conclusion -- References -- Architectures -- Increasing the Fault Tolerance of COTS FPGAs in Space: SEU Mitigation Techniques on MPSoC*-1pc -- 1 Introduction -- 2 Related Work -- 3 Development of Fault-Tolerance Techniques -- 3.1 HW/SW Fault-Tolerant Architecture -- 3.2 Coarse-Grained Application-Independent Redundancy -- 3.3 Fine-Grained Application-Specific Redundancy -- 3.4 Correction of Configuration Memory -- 4 Experimental Evaluation -- 4.1 Fault Injection and Evaluation Campaign -- 4.2 Experimental Results -- 5 Conclusion -- References -- Scalable and Energy-Efficient NN Acceleration with GPU-ReRAM Architecture -- 1 Introduction -- 2 Background: ReRAM for In-Memory NN Computing -- 3 Related Work -- 4 Proposed Architecture -- 4.1 Overall Architecture -- 4.2 GPU Layer -- 4.3 ReRAM Layer -- 4.4 Offloading: Selecting the Best Layers for ReRAM Acceleration -- 5 Evaluation Methodology -- 6 Results -- 6.1 Synthesis Results.
6.2 Computing Efficiency -- 6.3 Inference Accuracy -- 6.4 Energy Consumption -- 7 Conclusion and Future Work -- References -- On Guaranteeing Schedulability of Periodic Real-Time Hardware Tasks Under ReconOS64 -- 1 Introduction -- 2 Related Work -- 2.1 Real-Time Scheduling and Shared Resources on FPGAs -- 2.2 Operating Systems for FPGAs -- 2.3 Fixed-Priority Multi-processor Scheduling -- 3 System Architecture -- 4 Task Model and Runtime System -- 4.1 Task Model -- 4.2 Runtime System -- 5 Schedulability Analysis -- 6 Practical Example -- 6.1 Implementation Based on ReconOS64 -- 6.2 Exemplary Task Set -- 6.3 Applying the Schedulability Test -- 7 Conclusion and Future Work -- References -- Evolutionary FPGA-Based Spiking Neural Networks for Continual Learning*-1pc -- 1 Introduction -- 2 Learning Techniques for SNNs -- 3 The Proposed SNN-Based SoC Architecture -- 4 Proposed Learning Strategy -- 5 Data Encoding Strategy -- 6 Evaluation Setup -- 6.1 Iris Problem -- 6.2 Breast Cancer Wisconsin Dataset -- 6.3 Pima Indian Diabetes Dataset -- 6.4 Wine Dataset -- 6.5 The Mountain Car Environment -- 7 Experimental Results -- 7.1 Resource Utilization -- 7.2 Accuracy Results -- 8 Conclusions and Future Work -- References -- More Efficient CMMs on FPGAs: Instantiated Ternary Adders for Computation Coding -- 1 Introduction -- 2 Related Work -- 3 Computation Coding on FPGAs -- 3.1 Decomposition Algorithm -- 3.2 Hardware Designs -- 4 Hardware Generation Using Primitive Instantiation -- 4.1 Python Hardware

		Interface -- 4.2 TIAs on FPGAs -- 4.3 Primitive Generation -- 5 Evaluation -- 5.1 Setup -- 5.2 Comparison Between CMM Designs and SoA -- 6 Conclusion -- References -- Energy Efficient DNN Compaction for Edge Deployment -- 1 Introduction -- 2 Related Works -- 3 Proposed Approach -- 4 Experiments and Results -- 4.1 Experimental Setup -- 4.2 Results and Discussion. 5 Conclusion.
3.	Record Nr.	UNIORUON00495510
	Autore	CANTERA BURGOS, Francisco
	Titolo	Alvar García de Santa María y su familia de conversos : historia de la Judería de Burgos y de sus conversos más egregios / Francisco Cantera Burgos
	Pubbl/distr/stampa	Madrid, : Inst. Arias Montano, 1952
	Descrizione fisica	624 p. ; 25 cm.
	Disciplina	946
	Soggetti	SPAGNA - Storia
	Lingua di pubblicazione	Spagnolo
	Formato	Materiale a stampa
	Livello bibliografico	Monografia