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Nota di contenuto	Intro -- Organization -- Preface -- Plenary Talk -- Keynote Speeches -- Contents -- About the Editors -- Electronics -- Comparative Analysis of Static Bias Methods for Basic Differential Amplifier -- 1 Introduction -- 2 Circuit Description -- 3 Results and Discussion -- 4 Conclusion -- References -- Millimeter Wave Overmoded Circular Waveguide Tapers for ECRH Applications -- 1 Introduction -- 2 Theoretical Approach -- 3 Design Approaches -- 4 Simulation Outcome -- 4.1 Down Taper Ø (85 to 63.5) mm -- 4.2 Down Taper Ø (63.5 to 31.75) mm -- 5 Comparison and Discussion -- 6 Conclusion -- References -- Analysis of Logical Effort-Based Optimization in the Deep Submicron Technologies -- 1 Introduction -- 2 Determining the Optimum PMOS-To-NMOS Ratio -- 3 Logical Effort Method -- 3.1 Logical Effort Parameters [2] -- 3.2 Delay Optimization Using Logical Effort [2] -- 4 Logical Effort Parameters for 180 and 16 nm Technologies -- 4.1 Logical and Parasitic Effort of Different Gates -- 4.2 Defining -- 4.3 Delay Variation Due to Branching Effort (B) -- 4.4 Delay Variation Due to Parasitic Effort (P) -- 4.5 Delay Variation Due to Electrical Effort (H) -- 4.6 Comparison Between Electrical Effort (H) and Parasitic Effort (P) -- 4.7 Delay Variation Due to Logical Effort (G) -- 4.8 Delay Reduction Using Logic Effort-Based

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