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Collana	Theoretical Computer Science and General Issues, , 2512-2029 ; ; 5409
Disciplina	003.3
Soggetti	Computer systems Computer arithmetic and logic units Microprocessors Computer architecture Computer input-output equipment Logic design Computer networks Computer System Implementation Arithmetic and Logic Structures Processor Architectures Input/Output and Data Communications Logic Design Computer Communication Networks
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di contenuto	Invited Program -- Keynote: Challenges on the Road to Exascale Computing -- Keynote: Compilers in the Manycore Era -- I Dynamic Translation and Optimisation -- Steal-on-Abort: Improving Transactional Memory Performance through Dynamic Transaction Reordering -- Predictive Runtime Code Scheduling for Heterogeneous Architectures -- Collective Optimization -- High Speed CPU Simulation Using LTU Dynamic Binary Translation -- II Low Level Scheduling --

Integrated Modulo Scheduling for Clustered VLIW Architectures -- Software Pipelining in Nested Loops with Prolog-Epilog Merging -- A Flexible Code Compression Scheme Using Partitioned Look-Up Tables -- III Parallelism and Resource Control -- MLP-Aware Runahead Threads in a Simultaneous Multithreading Processor -- IPC Control for Multiple Real-Time Threads on an In-Order SMT Processor -- A Hardware Task Scheduler for Embedded Video Processing -- Finding Stress Patterns in Microprocessor Workloads -- IV Communication -- Deriving Efficient Data Movement from Decoupled Access/Execute Specifications -- MPSoC Design Using Application-Specific Architecturally Visible Communication -- Communication Based Proactive Link Power Management -- V Mapping for CMPs -- Mapping and Synchronizing Streaming Applications on Cell Processors -- Adapting Application Mapping to Systematic Within-Die Process Variations on Chip Multiprocessors -- Accomodating Diversity in CMPs with Heterogeneous Frequencies -- A Framework for Task Scheduling and Memory Partitioning for Multi-Processor System-on-Chip -- VI Power -- Hybrid Super/Subthreshold Design of a Low Power Scalable-Throughput FFT Architecture -- Predictive Thermal Management for Chip Multiprocessors Using Co-designed Virtual Machines -- HeDGE: Hybrid Dataflow Graph Execution in the Issue Logic -- Compiler Controlled Speculation for Power Aware ILP Extraction in Dataflow Architectures -- VII Cache Issues -- Revisiting Cache Block Superloading -- ACM: An Efficient Approach for Managing Shared Caches in Chip Multiprocessors -- In-Network Caching for Chip Multiprocessors -- VIII Parallel Embedded Applications -- Parallel LDPC Decoding on the Cell/B.E. Processor -- Parallel H.264 Decoding on an Embedded Multicore Processor.

Sommario/riassunto

This book constitutes the refereed proceedings of the Fourth International Conference on High Performance Embedded Architectures and Compilers, HiPEAC 2009, held in Paphos, Cyprus, in January 2009. The 27 revised full papers presented together with 2 invited keynote paper were carefully reviewed and selected from 97 submissions. The papers are organized in topical sections on dynamic translation and optimisation, low level scheduling, parallelism and resource control, communication, mapping for CMPs, power, cache issues as well as parallel embedded applications.