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Soggetti	Computers Operating systems (Computers) Software engineering Computer systems Computers, Special purpose Artificial intelligence Computer Hardware Operating Systems Software Engineering Computer System Implementation Special Purpose and Application-Based Systems Artificial Intelligence
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Nota di contenuto	Applications -- Fault-Tolerant Architecture for On-Board Dual-Core Synthetic-Aperture Radar Imaging -- Optimizing CNN-based Hyperspectral Image Classification on FPGAs -- Supporting Columnar In-Memory Formats on FPGA: The Hardware Design of Fletcher for Apache Arrow -- A Novel Encoder for TDCs -- A Resource Reduced Application-Specific FPGA Switch -- Software-Defined FPGA Accelerator Design for Mobile Deep Learning Applications -- Partial Reconfiguration and Security -- Probabilistic Performance Modelling

when using Partial Reconfiguration to Accelerate Streaming Applications with Non-Deterministic Task Scheduling -- Leveraging the Partial Reconfiguration Capability of FPGAs for Processor-Based Fail-Operational Systems -- (ReCo)Fuse Your PRC or Lose Security: Finally Reliable Reconfiguration-based Countermeasures on FPGAs -- Proof-Carrying Hardware versus the Stealthy Malicious LUT Hardware Trojan -- Secure Local Configuration of Intellectual Property Without a Trusted Third Party -- Image/Video Processing -- HiFlipVX: an Open Source High-Level Synthesis FPGA Library for Image Processing -- Real-time FPGA implementation of connected component labelling for a 4K video stream -- A Scalable FPGA-based Architecture for Depth Estimation in SLAM -- High-Level Synthesis -- Evaluating LULESH Kernels on OpenCL FPGA -- The TaPaSCo Open-Source Toolflow for the Automated Composition of Task-Based Parallel Reconfigurable Computing Systems -- Graph-based Code Restructuring Targeting HLS for FPGAs -- CGRAs and Vector Processing -- UltraSynth: Integration of a CGRA into a Control Engineering Environment -- Exploiting reconfigurable vector processing for energy-efficient computation in 3D-stacked memories -- Automatic Toolflow for VCGRA Generation to Enable CGRA Evaluation for Arithmetic Algorithms -- Architectures -- ReM: a Reconfigurable Multipotent Cell for New Distributed Reconfigurable Architectures -- Update or Invalidate: Influence of Coherence Protocols on Configurable HW Accelerators -- Design Frameworks and Methodology -- Hybrid Prototyping for Manycore Design and Validation -- Evaluation of FPGA Partitioning Schemes for Time and Space Sharing of Heterogeneous Tasks -- Invited Talk -- Third Party CAD Tools for FPGA Design | A Survey of the Current Landscape -- Convolutional Neural Networks -- Filter-wise Pruning Approach to FPGA Implementation of Fully Convolutional Network for Semantic Segmentation -- Exploring Data Size to Run Convolutional Neural Networks in Low Density FPGAs -- Faster Convolutional Neural Networks in Low Density FPGAs using Block Pruning.

Sommario/riassunto

This book constitutes the proceedings of the 15th International Symposium on Applied Reconfigurable Computing, ARC 2019, held in Darmstadt, Germany, in April 2019. The 20 full papers and 7 short papers presented in this volume were carefully reviewed and selected from 52 submissions. In addition, the volume contains 1 invited paper. The papers were organized in topical sections named: Applications; partial reconfiguration and security; image/video processing; high-level synthesis; CGRAs and vector processing; architectures; design frameworks and methodology; convolutional neural networks.