1. Record Nr. UNISA996466223603316

Titolo	Advances in Computer Systems Architecture [[electronic resource]] : 10th Asia-Pacific Conference, ACSAC 2005, Singapore, October 24-26, 2005, Proceedings / / edited by Thambipillai Srikanthan, Jingling Xue, Chip-Hong Chang
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2005
ISBN	3-540-32108-X 3-540-29643-3
Edizione	[1st ed. 2005.]
Descrizione fisica	1 online resource (XVIII, 834 p.)
Collana	Theoretical Computer Science and General Issues, , 2512-2029 ; ; 3740
Disciplina	004.2/2
Soggetti	Computer systems Computer arithmetic and logic units Computer input-output equipment Logic design Computer networks Microprocessors Computer architecture Computer System Implementation Arithmetic and Logic Structures Input/Output and Data Communications Logic Design Computer Communication Networks Processor Architectures
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Keynote Address I -- Processor Architecture for Trustworthy Computers -- Session 1A: Energy Efficient and Power Aware Techniques -- Efficient Voltage Scheduling and Energy-Aware Co-synthesis for Real-Time Embedded Systems -- Energy-Effective Instruction Fetch Unit for Wide Issue Processors -- Rule-Based Power-Balanced VLIW Instruction Scheduling with Uncertainty -- An Innovative

Instruction Cache for Embedded Processors -- Dynamic Voltage Scaling for Power Aware Fast Fourier Transform (FFT) Processor -- Session 1B: Methodologies and Architectures for Application-Specific Systems -- Design of an Efficient Multiplier-Less Architecture for Multi-dimensional Convolution -- A Pipelined Hardware Architecture for Motion Estimation of H.264/AVC -- Embedded Intelligent Imaging On-Board Small Satellites -- Architectural Enhancements for Color Image and Video Processing on Embedded Systems -- A Portable Doppler Device Based on a DSP with High- Performance Spectral Estimation and Output -- Session 2A: Processor Architectures and Microarchitectures -- A Power-Efficient Processor Core for Reactive Embedded Applications -- A Stream Architecture Supporting Multiple Stream Execution Models -- The Challenges of Massive On-Chip Concurrency -- FMRPU: Design of Fine-Grain Multi-context Reconfigurable Processing Unit -- Session 2B: High-Reliability and Fault-Tolerant Architectures -- Modularized Redundant Parallel Virtual File System -- Resource-Driven Optimizations for Transient-Fault Detecting SuperScalar Microarchitectures -- A Fault-Tolerant Routing Strategy for Fibonacci-Class Cubes -- Embedding of Cycles in the Faulty Hypercube -- Session 3A: Compiler and OS for Emerging Architectures -- Improving the Performance of GCC by Exploiting IA-64 Architectural Features -- An Integrated Partitioning and Scheduling Based Branch Decoupling -- A Register Allocation Framework for Banked Register Files with Access Constraints -- Designing a Concurrent Hardware Garbage Collector for Small Embedded Systems -- Irregular Redistribution Scheduling by Partitioning Messages -- Session 3B: Data Value Predictions -- Making Power-Efficient Data Value Predictions -- Speculative Issue Logic -- Using Decision Trees to Improve Program-Based and Profile-Based Static Branch Prediction -- Arithmetic Data Value Speculation -- Exploiting Thread-Level Speculative Parallelism with Software Value Prediction -- Keynote Address II -- Challenges and Opportunities on Multi-core Microprocessor -- Session 4A: Reconfigurable Computing Systems and Polymorphic Architectures -- Software-Oriented System-Level Simulation for Design Space Exploration of Reconfigurable Architectures -- A Switch Wrapper Design for SNA On-Chip-Network -- A Configuration System Architecture Supporting Bit-Stream Compression for FPGAs -- Biological Sequence Analysis with Hidden Markov Models on an FPGA -- FPGAs for Improved Energy Efficiency in Processor Based Systems -- Morphable Structures for Reconfigurable Instruction Set Processors -- Session 4B: Interconnect Networks and Network Interfaces -- Implementation of a Hybrid TCP/IP Offload Engine Prototype -- Matrix-Star Graphs: A New Interconnection Network Based on Matrix Operations -- The Channel Assignment Algorithm on RP(k) Networks -- Extending Address Space of IP Networks with Hierarchical Addressing -- The Star-Pyramid Graph: An Attractive Alternative to the Pyramid -- Building a Terabit Router with XD Networks -- Session 5A: Parallel Architectures and Computation Models -- A Real Coded Genetic Algorithm for Data Partitioning and Scheduling in Networks with Arbitrary Processor Release Time -- D3DPR: A Direct3D-Based Large-Scale Display Parallel Rendering System Architecture for Clusters -- Determining Optimal Grain Size for Efficient Vector Processing on SIMD Image Processing Architectures -- A Technique to Reduce Preemption Overhead in Real-Time Multiprocessor Task Scheduling -- Session 5B: Hardware-Software Partitioning, Verification, and Testing of Complex Architectures -- Minimizing Power in Hardware/Software Partitioning -- Exploring Design Space Using Transaction Level Models -- Increasing Embedding Probabilities of RPRPs in RIN Based BIST -- A

Practical Test Scheduling Using Network-Based TAM in Network on Chip Architecture -- Session 6A: Architectures for Secured Computing -- DRIL– A Flexible Architecture for Blowfish Encryption Using Dynamic Reconfiguration, Replication, Inner-Loop Pipelining, Loop Folding Techniques -- Efficient Architectural Support for Secure Bus-Based Shared Memory Multiprocessor -- Covert Channel Analysis of the Password-Capability System -- Session 6B: Simulation and Performance Evaluation -- Comparing Low-Level Behavior of SPEC CPU and Java Workloads -- Application of Real-Time Object-Oriented Modeling Technique for Real-Time Computer Control -- VLSI Performance Evaluation and Analysis of Systolic and Semisystolic Finite Field Multipliers -- Session 7: Architectures for Emerging Technologies and Applications I -- Analysis of Real-Time Communication System with Queuing Priority -- FPGA Implementation and Analyses of Cluster Maintenance Algorithms in Mobile Ad-Hoc Networks -- A Study on the Performance Evaluation of Forward Link in CDMA Mobile Communication Systems -- Session 8: Memory Systems Hierarchy and Management -- Cache Leakage Management for Multi-programming Workloads -- A Memory Bandwidth Effective Cache Store Miss Policy -- Application-Specific Hardware-Driven Prefetching to Improve Data Cache Performance -- Targeted Data Prefetching -- Session 9: Architectures for Emerging Technologies and Applications II -- Area-Time Efficient Systolic Architecture for the DCT -- Efficient VLSI Architectures for Convolution and Lifting Based 2-D Discrete Wavelet Transform -- A Novel Reversible TSG Gate and Its Application for Designing Reversible Carry Look-Ahead and Other Adder Architectures -- Implementation and Analysis of TCP/IP Offload Engine and RDMA Transfer Mechanisms on an Embedded System.

Sommario/riassunto

On behalf of the ProgramCommittee, we are pleased to present the proceedings of the 2005 Asia-Paci?c Computer Systems Architecture Conference (ACSAC 2005) held in the beautiful and dynamic country of Singapore. This conference was the tenth in its series, one of the leading forums for sharing the emerging research ?ndings in this ?eld. In consultation with the ACSAC Steering Committee, we selected a - member Program Committee. This Program Committee represented a broad spectrum of research expertise to ensure a good balance of research areas, - stitutions and experience while maintaining the high quality of this conference series. This year’s committee was of the same size as last year but had 19 new faces. We received a total of 173 submissions which is 14% more than last year. Each paper was assigned to at least three and in some cases four ProgramC- mittee members for review. Wherever necessary, the committee members called upon the expertise of their colleagues to ensure the highest possible quality in the reviewing process. As a result, we received 415 reviews from the Program Committee members and their 105 co-reviewers whose names are acknowledged inthe proceedings.Theconferencecommitteeadopteda systematicblind review process to provide a fair assessment of all submissions. In the end, we accepted 65 papers on a broad range of topics giving an acceptance rate of 37.5%. We are grateful to all the Program Committee members and the co-reviewers for their e?orts in completing the reviews within a tight schedule.

2.

Record Nr.	UNISANNIOUFI0209029
Autore	Taddei, Francesca
Titolo	Il Pignone di Firenze : 1944-1954 / di Francesca Taddei ; con un saggio di Lirio Mangalaviti: Il Pignone tra Resistenza e ricostruzione
Pubbl/distr/stampa	Firenze, : La nuova Italia, 1980
Descrizione fisica	144 p. ; 18 cm.
Collana	Toscana-sindacato ; 3
Classificazione	IT/2724.3/TOS IT/2724.7 IT/3432.9 IT/3436.5 TOS/25.3/FI TOS/35.3/FI
Disciplina	331.88 331.880945
Soggetti	Firenze - Pignone - Vertenze sindacali - 1944-1954
Collocazione	POZZO LIB.F. SANTI 381
Lingua di pubblicazione	Italiano
Formato	Materiale a stampa
Livello bibliografico	Monografia

3. Record Nr. UNINA9910633930503321

Titolo	Formal Methods: Foundations and Applications : 25th Brazilian Symposium, SBMF 2022, Virtual Event, December 6–9, 2022, Proceedings / / edited by Lucas Lima, Vince Molnár
Pubbl/distr/stampa	Cham : , : Springer International Publishing : , : Imprint : Springer, , 2022
ISBN	9783031224768 3031224760
Edizione	[1st ed. 2022.]
Descrizione fisica	1 online resource (154 pages)
Collana	Lecture Notes in Computer Science, , 1611-3349 ; ; 13768
Disciplina	005.1
Soggetti	Software engineering Natural language processing (Computer science) Logic programming Computer science Computers, Special purpose Computer networks Software Engineering Natural Language Processing (NLP) Logic in AI Theory of Computation Special Purpose and Application-Based Systems Computer Communication Networks
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Invited Talks -- Model Checking and Semantics -- Generation and Synthesis -- Verification and Solvers.
Sommario/riassunto	This book constitutes the refereed proceedings of the 25th Brazilian Symposium on Formal Methods, SBMF 2022, which was held virtually in December 2022. The 8 regular papers presented in this book were carefully reviewed and selected from 15 submissions. The symposium focuses on the development, dissemination, and use of formal methods for the construction of high-quality computational systems, aiming to

promote opportunities for researchers and practitioners with an interest in formal methods to discuss the recent advances in this area. .