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Nota di contenuto	Keynote Address I -- Processor Architecture for Trustworthy Computers -- Session 1A: Energy Efficient and Power Aware Techniques -- Efficient Voltage Scheduling and Energy-Aware Co-synthesis for Real-Time Embedded Systems -- Energy-Effective Instruction Fetch Unit for Wide Issue Processors -- Rule-Based Power-Balanced VLIW Instruction Scheduling with Uncertainty -- An Innovative

Instruction Cache for Embedded Processors -- Dynamic Voltage Scaling for Power Aware Fast Fourier Transform (FFT) Processor -- Session 1B: Methodologies and Architectures for Application-Specific Systems -- Design of an Efficient Multiplier-Less Architecture for Multi-dimensional Convolution -- A Pipelined Hardware Architecture for Motion Estimation of H.264/AVC -- Embedded Intelligent Imaging On-Board Small Satellites -- Architectural Enhancements for Color Image and Video Processing on Embedded Systems -- A Portable Doppler Device Based on a DSP with High- Performance Spectral Estimation and Output -- Session 2A: Processor Architectures and Microarchitectures -- A Power-Efficient Processor Core for Reactive Embedded Applications -- A Stream Architecture Supporting Multiple Stream Execution Models -- The Challenges of Massive On-Chip Concurrency -- FMRPU: Design of Fine-Grain Multi-context Reconfigurable Processing Unit -- Session 2B: High-Reliability and Fault-Tolerant Architectures -- Modularized Redundant Parallel Virtual File System -- Resource-Driven Optimizations for Transient-Fault Detecting SuperScalar Microarchitectures -- A Fault-Tolerant Routing Strategy for Fibonacci-Class Cubes -- Embedding of Cycles in the Faulty Hypercube -- Session 3A: Compiler and OS for Emerging Architectures -- Improving the Performance of GCC by Exploiting IA-64 Architectural Features -- An Integrated Partitioning and Scheduling Based Branch Decoupling -- A Register Allocation Framework for Banked Register Files with Access Constraints -- Designing a Concurrent Hardware Garbage Collector for Small Embedded Systems -- Irregular Redistribution Scheduling by Partitioning Messages -- Session 3B: Data Value Predictions -- Making Power-Efficient Data Value Predictions -- Speculative Issue Logic -- Using Decision Trees to Improve Program-Based and Profile-Based Static Branch Prediction -- Arithmetic Data Value Speculation -- Exploiting Thread-Level Speculative Parallelism with Software Value Prediction -- Keynote Address II -- Challenges and Opportunities on Multi-core Microprocessor -- Session 4A: Reconfigurable Computing Systems and Polymorphic Architectures -- Software-Oriented System-Level Simulation for Design Space Exploration of Reconfigurable Architectures -- A Switch Wrapper Design for SNA On-Chip-Network -- A Configuration System Architecture Supporting Bit-Stream Compression for FPGAs -- Biological Sequence Analysis with Hidden Markov Models on an FPGA -- FPGAs for Improved Energy Efficiency in Processor Based Systems -- Morphable Structures for Reconfigurable Instruction Set Processors -- Session 4B: Interconnect Networks and Network Interfaces -- Implementation of a Hybrid TCP/IP Offload Engine Prototype -- Matrix-Star Graphs: A New Interconnection Network Based on Matrix Operations -- The Channel Assignment Algorithm on $RP(k)$ Networks -- Extending Address Space of IP Networks with Hierarchical Addressing -- The Star-Pyramid Graph: An Attractive Alternative to the Pyramid -- Building a Terabit Router with XD Networks -- Session 5A: Parallel Architectures and Computation Models -- A Real Coded Genetic Algorithm for Data Partitioning and Scheduling in Networks with Arbitrary Processor Release Time -- D3DPR: A Direct3D-Based Large-Scale Display Parallel Rendering System Architecture for Clusters -- Determining Optimal Grain Size for Efficient Vector Processing on SIMD Image Processing Architectures -- A Technique to Reduce Preemption Overhead in Real-Time Multiprocessor Task Scheduling -- Session 5B: Hardware-Software Partitioning, Verification, and Testing of Complex Architectures -- Minimizing Power in Hardware/Software Partitioning -- Exploring Design Space Using Transaction Level Models -- Increasing Embedding Probabilities of RPRPs in RIN Based BIST -- A

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Sommario/riassunto

On behalf of the Program Committee, we are pleased to present the proceedings of the 2005 Asia-Pacific Computer Systems Architecture Conference (ACSAC 2005) held in the beautiful and dynamic country of Singapore. This conference was the tenth in its series, one of the leading forums for sharing the emerging research findings in this field. In consultation with the ACSAC Steering Committee, we selected a 7-member Program Committee. This Program Committee represented a broad spectrum of research expertise to ensure a good balance of research areas, institutions and experience while maintaining the high quality of this conference series. This year's committee was of the same size as last year but had 19 new faces. We received a total of 173 submissions which is 14% more than last year. Each paper was assigned to at least three and in some cases four Program Committee members for review. Wherever necessary, the committee members called upon the expertise of their colleagues to ensure the highest possible quality in the reviewing process. As a result, we received 415 reviews from the Program Committee members and their 105 co-reviewers whose names are acknowledged in the proceedings. The conference committee adopted a systematic blind review process to provide a fair assessment of all submissions. In the end, we accepted 65 papers on a broad range of topics giving an acceptance rate of 37.5%. We are grateful to all the Program Committee members and the co-reviewers for their efforts in completing the reviews within a tight schedule.
