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Autore	Suleiman Ezra
Titolo	Dismantling democratic states // Ezra Suleiman
Pubbl/distr/stampa	Princeton, New Jersey : , : Princeton University Press, , 2003 ©2003
ISBN	0-691-11534-6 1-4008-5073-8
Edizione	[Course Book]
Descrizione fisica	1 online resource (342 p.)
Disciplina	321.8
Soggetti	Organizational change Administrative agencies - Reorganization Privatization Bureaucracy Democracy Electronic books.
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Includes index.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Frontmatter -- Contents -- Acknowledgments -- Introduction -- Chapter 1. The End of Bureaucracy? -- Chapter 2. Beyond Weber? -- Chapter 3. New Conceptions of Bureaucracy, Democracy, and Citizenship -- Chapter 4. Popular Dissatisfaction and Administrative Reform -- Chapter 5. Universalistic Reforms -- Chapter 6. Emulating the Private Sector -- Chapter 7. The Reluctant Reformers: Japan and France -- Chapter 8. Deprofessionalization: The Decline of the Civil Service Career -- Chapter 9. Deprofessionalization: The Process of Politicization -- Chapter 10. The End of the Nonpolitical Bureaucracy -- Chapter 11. Constructing a Bureaucratic Apparatus in East-Central Europe -- Chapter 12. The Politics of Bureaucratic Reform -- Index
Sommario/riassunto	Bureaucracy is a much-maligned feature of contemporary government. And yet the aftermath of September 11 has opened the door to a reassessment of the role of a skilled civil service in the survival and viability of democratic society. Here, Ezra Suleiman offers a timely and powerful corrective to the widespread view that bureaucracy is the

source of democracy's ills. This is a book as much about good governance as it is about bureaucratic organizations. Suleiman asks: Is democratic governance hindered without an effective instrument in the hands of the legitimately elected political leadership? Is a professional bureaucracy required for developing but not for maintaining a democratic state? Why has a reform movement arisen in recent years championing the gradual dismantling of bureaucracy, and what are the consequences? Suleiman undertakes a comparative analysis of the drive toward a civil service grounded in the New Public Management. He argues that "government reinvention" has limited bureaucracy's capacity to adequately serve the public good. All bureaucracies have been under political pressure in recent years to reduce not only their size but also their effectiveness, and all have experienced growing deprofessionalism and politicization. He compares the impact of this evolution in both democratic societies and societies struggling to consolidate democratic institutions. Dismantling Democratic States cautions that our failure to acknowledge the role of an effective bureaucracy in building and preserving democratic political systems threatens the survival of democracy itself.

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2. Record Nr.	UNISA996466181903316
Titolo	Formal methods in computer-aided design : third international conference, FMCAD 2000, Austin, TX, USA, November 1-3, 2000 : proceedings / / edited by Warren A. Hunt. Steven D. Johnson
Pubbl/distr/stampa	Berlin, Germany ; ; New York, New York : , : Springer, , [2000] Â©2000
ISBN	3-540-40922-X
Edizione	[1st ed. 2000.]
Descrizione fisica	1 online resource (XII, 552 p.)
Collana	Lecture Notes in Computer Science, , 0302-9743 ; ; 1954
Disciplina	621.392
Soggetti	Computer engineering - Computer-aided design Integrated circuits - Verification
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Includes index.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Applications of Hierarchical Verification in Model Checking -- Applications of Hierarchical Verification in Model Checking -- Invited Talk -- Trends in Computing -- Invited Paper -- A Case Study in Formal Verification of Register-Transfer Logic with ACL2: The Floating Point Adder of the AMD Athlon TM Processor -- Contributed Papers -- An Algorithm for Strongly Connected Component Analysis in $n \log n$ Symbolic Steps -- Automated Refinement Checking for Asynchronous Processes -- Border-Block Triangular Form and Conjunction Schedule in Image Computation -- B2M: A Semantic Based Tool for BLIF Hardware Descriptions -- Checking Safety Properties Using Induction and a SAT-Solver -- Combining Stream-Based and State-Based Verification Techniques -- A Comparative Study of Symbolic Algorithms for the Computation of Fair Cycles -- Correctness of Pipelined Machines -- Do You Trust Your Model Checker? -- Executable Protocol Specification in ESL -- Formal Verification of Floating Point Trigonometric Functions -- Hardware Modeling Using Function Encapsulation -- A Methodology for the Formal Analysis of Asynchronous Micropipelines -- A Methodology for Large-Scale Hardware Verification -- Model Checking Synchronous Timing Diagrams -- Model Reductions and a Case Study -- Modeling and Parameters Synthesis for an Air TrafficManagement System -- Monitor-

Based Formal Specification of PCI -- SAT-Based Image Computation with Application in Reachability Analysis -- SAT-Based Verification without State Space Traversal -- Scalable Distributed On-the-Fly Symbolic Model Checking -- The Semantics of Verilog Using Transition System Combinators -- Sequential Equivalence Checking by Symbolic Simulation -- Speeding Up Image Computation by Using RTL Information -- Symbolic Checking of Signal-Transition Consistency for Verifying High-Level Designs -- Symbolic Simulation with Approximate Values -- A Theory of Consistency for Modular Synchronous Systems -- Verifying Transaction Ordering Properties in Unbounded Bus Networks through Combined Deductive/Algorithmic Methods -- Visualizing System Factorizations with Behavior Tables.

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## Sommario/riassunto

The biannual Formal Methods in Computer Aided Design conference (FMCAD 2000) is the third in a series of conferences under that title devoted to the use of discrete mathematical methods for the analysis of computer hardware and software. The work reported in this book describes the use of modeling languages and their associated automated analysis tools to specify and verify computing systems. Functional verification has become one of the principal costs in a modern computer design effort. In addition, verification of circuit models, timing, power, etc., requires even more effort. FMCAD provides a venue for academic and industrial researchers and practitioners to share their ideas and experiences of using discrete mathematical modeling and verification. It is noted with interest by the conference chairmen how this area has grown from just a few people 15 years ago to a vibrant area of research, development, and deployment. It is clear that these methods are helping reduce the cost of designing computing systems. As an example of this potential cost reduction, we have invited David Russino of Advanced Micro Devices, Inc. to describe his verification of floating-point algorithms being used in AMD microprocessors. The program includes 30 regular presentations selected from 63 submitted papers.

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