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Collana	Lecture Notes in Computer Science, , 0302-9743 ; ; 987
Disciplina	621.39/5
Soggetti	Architecture, Computer Electronics Microelectronics Input-output equipment (Computers) Software engineering Computer logic Computer System Implementation Electronics and Microelectronics, Instrumentation Input/Output and Data Communications Software Engineering Logics and Meanings of Programs
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Nota di contenuto	What if model checking must be truly symbolic -- Automatic verification of the SCI cache coherence protocol -- Describing and verifying synchronous circuits with the Boyer-Moore theorem prover -- Problems encountered in the machine-assisted proof of hardware -- Formally embedding existing high level synthesis algorithms -- Formal design of a class of computers — its high stage: abstract microprogramming -- Symbolic analysis and verification of CPA descriptions -- A foundation for formal reuse of hardware -- State enumeration with abstract descriptions of state machines -- Transforming Boolean relations by symbolic encoding -- Design error

diagnosis in sequential circuits -- Timing analysis of asynchronous circuits using timed automata -- Improved probabilistic verification by hash compaction -- Formal support for the ELLA hardware description language -- Verifying hardware components with JACK -- Language containment of non-deterministic ?-automata -- A partial-order approach to the verification of concurrent systems: Checking liveness properties -- Semantics of a verification-oriented subset of VHDL -- Reasoning about VHDL using operational and observational semantics -- A symbolic relation for a subset of VHDL'87 descriptions and its application to symbolic model checking.

Sommario/riassunto

This book constitutes the refereed proceedings of the IFIP WG10.5 Advanced Research Working Conference on Correct Hardware Design Methodologies, CHARME '95, held in Frankfurt, Germany, in October 1995. The 20 revised full papers presented were carefully selected by the program committee and address all current aspects of research and advanced applications in the field of formal verification of hardware. Among the topics covered are model checking, theorem proving, formally verified synthesis, process algebras, finite state systems, verification environments, language containment, and VHDL.