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Disciplina	621.39/2
Soggetti	Computers Computer hardware Microprogramming Arithmetic and logic units, Computer Computer memory systems Input-output equipment (Computers) Theory of Computation Computer Hardware Control Structures and Microprogramming Arithmetic and Logic Structures Memory Structures Input/Output and Data Communications
Lingua di pubblicazione	Inglese
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Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di contenuto	A graph-based method for timing diagrams representation and verification -- A Petri Net approach for the analysis of VHDL descriptions -- Temporal analysis of time bounded digital systems -- Strongly-typed theory of structures and behaviours -- Verification and diagnosis of digital systems by ternary reasoning -- Logic verification of incomplete functions and design error location -- A methodology for system-level design for verifiability -- Algebraic models and the correctness of microprocessors -- Combining symbolic evaluation and

object oriented approach for verifying processor-like architectures at the RT-level -- A theory of generic interpreters -- Towards verifying large(r) systems: A strategy and an experiment -- Advancements in symbolic traversal techniques -- Automatic verification of speed-independent circuit designs using the Circal system -- Correct compilation of specifications to deterministic asynchronous circuits -- DDD-FM9001: Derivation of a verified microprocessor -- Calculational derivation of a counter with bounded response time -- Towards a provably correct hardware implementation of occam -- Rewriting with constraints in T-ruby -- Embedding hardware verification within a commercial design framework -- An approach to formalization of data flow graphs.

Sommario/riassunto

These proceedings contain the papers presented at the Advanced Research Working Conference on Correct Hardware Design Methodologies, held in Arles, France, in May 1993, and organized by the ESPRIT Working Group 6018 CHARME-2and the Universit de Provence, Marseille, in cooperation with IFIP Working Group 10.2. Formal verification is emerging as a plausible alternative to exhaustive simulation for establishing correct digital hardware designs. The validation of functional and timing behavior is a major bottleneck in current VLSI design systems, slowing the arrival of products in the marketplace with its associated increase in cost. From being a predominantly academic area of study until a few years ago, formal design and verification techniques are now beginning to migrate into industrial use. As we are now witnessing an increase in activity in this area in both academia and industry, the aim of this working conference was to bring together researchers and users from both communities.