

1. Record Nr.	UNISA996466078003316
Titolo	Computer Aided Verification [[electronic resource] ] : Fourth International Workshop, CAV '92, Montreal, Canada, June 29 - July 1, 1992. Proceedings // edited by Gregor von Bochmann, David K. Probst
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 1993
ISBN	3-540-47572-9
Edizione	[1st ed. 1993.]
Descrizione fisica	1 online resource (IX, 426 p.)
Collana	Lecture Notes in Computer Science, , 0302-9743 ; ; 663
Disciplina	005.1015113
Soggetti	Computer logic Operating systems (Computers) Software engineering Electronics Microelectronics Mathematical logic Logics and Meanings of Programs Operating Systems Software Engineering/Programming and Operating Systems Software Engineering Electronics and Microelectronics, Instrumentation Mathematical Logic and Foundations
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di contenuto	Computer-hindered verification (humans can do it too) -- Modular abstractions for verifying real-time distributed systems -- Layering techniques for development of parallel systems -- Efficient local correctness checking -- Mechanical verification of concurrent systems with TLA -- Using a theorem prover for reasoning about concurrent algorithms -- Verifying a logic synthesis tool in Nuprl: A case study in software verification -- Higher-level specification and verification with BDDs -- Symbolic bisimulation minimisation -- Towards a verification technique for large synchronous circuits -- Verifying timed behavior

automata with nonbinary delay constraints -- Timing verification by successive approximation -- A verification strategy for timing constrained systems -- Using unfoldings to avoid the state explosion problem in the verification of asynchronous circuits -- State space caching revisited -- Verification in process algebra of the distributed control of track vehicles—A case study -- Design verification of a microprocessor using branching time regular temporal logic -- A case study in safety-critical design -- Automatic reduction in CTL compositional model checking -- Compositional model checking for linear-time temporal logic -- Property preserving simulations -- Verification with real-time COSPAN -- Model-checking for real-time systems specified in Lotos -- Decidability of bisimulation equivalences for parallel timer processes -- A proof assistant for symbolic model-checking -- Tableau recycling -- Crocos: An integrated environment for interactive verification of SDL specifications -- Verifying general safety and liveness properties with integer programming -- Generating diagnostic information for behavioral preorders -- A verification procedure via invariant for extended communicating finite-state machines -- Efficient  $\omega$ -regular language containment -- Faster model checking for the modal  $\mu$ -Calculus.

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### Sommario/riassunto

This volume gives the proceedings of the Fourth Workshop on Computer-Aided Verification (CAV '92), held in Montreal, June 29 - July 1, 1992. The objective of this series of workshops is to bring together researchers and practitioners interested in the development and use of methods, tools and theories for the computer-aided verification of concurrent systems. The workshops provide an opportunity for comparing various verification methods and practical tools that can be used to assist the applications designer. Emphasis is placed on new research results and the application of existing results to real verification problems. The volume contains 31 papers selected from 75 submissions. These are organized into parts on reduction techniques, proof checking, symbolic verification, timing verification, partial-order approaches, case studies, model and proof checking, and other approaches. The volume starts with an invited lecture by Leslie Lamport entitled "Computer-hindered verification (humans can do it too)".

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