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Nota di contenuto	Invited Papers -- High Performance Computing Trends and Self Adapting Numerical Software -- Kilo-instruction Processors -- CARE: Overview of an Adaptive Multithreaded Architecture -- Numerical Simulator III – A Terascale SMP-Cluster System for Aerospace Science and Engineering: Its Design and the Performance Issue -- Award Papers -- Code and Data Transformations for Improving Shared Cache Performance on SMT Processors -- Improving Memory Latency Aware Fetch Policies for SMT Processors -- Architecture -- Tolerating Branch

Predictor Latency on SMT -- A Simple Low-Energy Instruction Wakeup Mechanism -- Power-Performance Trade-Offs in Wide and Clustered VLIW Cores for Numerical Codes -- Field Array Compression in Data Caches for Dynamically Allocated Recursive Data Structures -- Software -- FIBER: A Generalized Framework for Auto-tuning Software -- Evaluating Heuristic Scheduling Algorithms for High Performance Parallel Processing -- Pursuing Laziness for Efficient Implementation of Modern Multithreaded Languages -- SPEC HPG Benchmarks for Large Systems -- Applications -- Distribution-Insensitive Parallel External Sorting on PC Clusters -- Distributed Genetic Algorithm for Inference of Biological Scale-Free Network Structure -- Is Cook's Theorem Correct for DNA-Based Computing? -- LES of Unstable Combustion in a Gas Turbine Combustor -- ITBL -- Grid Computing Supporting System on ITBL Project -- A Visual Resource Integration Environment for Distributed Applications on the ITBL System -- Development of Remote Visualization and Collaborative Visualization System in ITBL Grid Environment -- Performance of Network Intrusion Detection Cluster System -- Constructing a Virtual Laboratory on the Internet: The ITBL Portal -- Evaluation of High-Speed VPN Using CFD Benchmark -- The Development of the UPACS CFD Environment -- Virtual Experiment Platform for Materials Design -- Ab Initio Study of Hydrogen Hydrate Clathrates for Hydrogen Storage within the ITBL Environment -- Short Papers -- RI2N – Interconnection Network System for Clusters with Wide-Bandwidth and Fault-Tolerancy Based on Multiple Links -- A Bypass-Sensitive Blocking-Preventing Scheduling Technique for Mesh-Connected Multicomputers -- Broadcast in a MANET Based on the Beneficial Area -- An Optimal Method for Coordinated En-route Web Object Caching -- An Improved Algorithm of Multicast Topology Inference from End-to-End Measurements -- Chordal Topologies for Interconnection Networks -- Distributed Location of Shared Resources and Its Application to the Load Sharing Problem in Heterogeneous Distributed Systems -- Design and Implementation of a Parallel Programming Environment Based on Distributed Shared Arrays -- Design and Implementation of Parallel Modified PrefixSpan Method -- Parallel LU-decomposition on Pentium Streaming SIMD Extensions -- Parallel Matrix Multiplication and LU Factorization on Ethernet-Based Clusters -- Online Remote Trace Analysis of Parallel Applications on High-Performance Clusters -- Performance Study of a Whole Genome Comparison Tool on a Hyper-Threading Multiprocessor -- The GSN Library and FORTRAN Level I/O Benchmarks on the NS-III HPC System -- Large Scale Structures of Turbulent Shear Flow via DNS -- Molecular Dynamics Simulation of Prion Protein by Large Scale Cluster Computing -- International Workshop on OpenMP: Experiences and Implementations (WOMPEI 2003) -- OpenMP/MPI Hybrid vs. Flat MPI on the Earth Simulator: Parallel Iterative Solvers for Finite Element Method -- Performance Evaluation of Low Level Multithreaded BLAS Kernels on Intel Processor Based cc-NUMA Systems -- Support of Multidimensional Parallelism in the OpenMP Programming Model -- On the Implementation of OpenMP 2.0 Extensions in the Fujitsu PRIMEPOWER Compiler -- Improve OpenMP Performance by Extending BARRIER and REDUCTION Constructs -- OpenMP for Adaptive Master-Slave Message Passing Applications -- OpenGR: A Directive-Based Grid Programming Environment.

Sommario/riassunto

The 5th International Symposium on High Performance Computing (ISHPC–V) was held in Odaiba, Tokyo, Japan, October 20–22, 2003. The symposium was thoughtfully planned, organized, and supported by the ISHPC Organizing C- mittee and its collaborating organizations. The ISHPC-V program included two keynote speeches, several invited talks,

two panel discussions, and technical sessions covering theoretical and applied research topics in high–performance computing and representing both academia and industry. One of the regular sessions highlighted the research results of the ITBL project (IT–based research laboratory, http://www.itbl.riken.go.jp/). ITBL is a Japanese national project started in 2001 with the objective of re- izing a virtual joint research environment using information technology. ITBL aims to connect 100 supercomputers located in main Japanese scienti?c research laboratories via high–speed networks. A total of 58 technical contributions from 11 countries were submitted to ISHPC-V. Each paper received at least three peer reviews. After a thorough evaluation process, the program committee selected 14 regular (12-page) papers for presentation at the symposium. In addition, several other papers with fav- able reviews were recommended for a poster session presentation. They are also included in the proceedings as short (8-page) papers.

Theprogramcommitteegaveadistinguishedpaperawardandabeststudent paper award to two of the regular papers. The distinguished paper award was given for “Code and Data Transformations for Improving Shared Cache P- formance on SMT Processors” by Dimitrios S. Nikolopoulos. The best student paper award was given for “Improving Memory Latency Aware Fetch Policies for SMT Processors” by Francisco J. Cazorla.