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	Nota di contenuto	The formal architecture model -- Functional modules -- Hardwired control -- Design of a minimal CPU -- Design of the DLX machine -- Trade-off analyses -- Interrupt -- Microprogrammed control -- Further applications of the architecture model.
	Sommario/riassunto	This book presents a formal model for evaluating the cost effectiveness of computer architectures. The model can cope with a wide range of architectures, from CPU design to parallel supercomputers. To illustrate the formal procedure of trade-off analyses, several non-pipelined design alternatives for the well-known RISC architecture called DLX are

analyzed quantitatively. It is formally proved that the interrupt mechanism proposed for the DLX architecture handles nested interrupts correctly. In an appendix all programs to compute the cost and cycle time of the designs described are listed in C code. Running these simple C programs on a PC is sufficient to verify the results presented. The book addresses design professionals and students in computer architecture.