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Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Keynote I -- Compilation Techniques for Partitioned Global Address Space Languages -- Session 1: Programming Models -- Can Transactions Enhance Parallel Programs? -- Design and Use of htalib – A Library for Hierarchically Tiled Arrays -- SP@CE - An SP-Based Programming Model for Consumer Electronics Streaming Applications -- Session 2: Code Generation -- Data Pipeline Optimization for Shared

Memory Multiple-SIMD Architecture -- Dependence-Based Code Generation for a CELL Processor -- Expression and Loop Libraries for High-Performance Code Synthesis -- Applying Code Specialization to FFT Libraries for Integral Parameters -- Session 3: Parallelism -- A Characterization of Shared Data Access Patterns in UPC Programs -- Exploiting Speculative Thread-Level Parallelism in Data Compression Applications -- On Control Signals for Multi-Dimensional Time -- Keynote II -- The Berkeley View: A New Framework and a New Platform for Parallel Research -- Session 4: Compilation Techniques -- An Effective Heuristic for Simple Offset Assignment with Variable Coalescing -- Iterative Compilation with Kernel Exploration -- Quantifying Uncertainty in Points-To Relations -- Session 5: Data Structures -- Cache Behavior Modelling for Codes Involving Banded Matrices -- Tree-Traversal Orientation Analysis -- UTS: An Unbalanced Tree Search Benchmark -- Session 6: Register Allocation -- Copy Propagation Optimizations for VLIW DSP Processors with Distributed Register Files -- Optimal Bitwise Register Allocation Using Integer Linear Programming -- Register Allocation: What Does the NP-Completeness Proof of Chaitin et al. Really Prove? Or Revisiting Register Allocation: Why and How -- Session 7: Memory Management -- Custom Memory Allocation for Free -- Optimizing the Use of Static Buffers for DMA on a CELL Chip -- Runtime Address Space Computation for SDSM Systems -- A Static Heap Analysis for Shape and Connectivity: Unified Memory Analysis: The Base Framework.

Sommario/riassunto

The 19th Workshop on Languages and Compilers for Parallel Computing was heldinNovember2006inNewOrleans,LouisianaUSA. Morethan40researchers from around the world gathered together to present their latest results and to exchange ideas on topics ranging from parallel programming models, code generation, compilationtechniques,paralleldatastructureandparallelexecution models, toregisterallocationandmemorymanagementinparallelenvironments. Out of the 49 paper submissions, the Program Committee, with the help of external reviewers, selected 24 papers for presentation at the workshop. Each paper had at least three reviews and was extensively discussed in the comm- tee meeting. The papers were presented in 30-minute sessions at the workshop. One of the selected papers, while still included in the proceedings, was not p- sented because of an unfortunate visa problem that prevented the authors from attending the workshop. We werefortunateto havetwooutstanding keynoteaddressesatLCPC2006, both from UC Berkeley. Kathy Yelick presented “Compilation Techniques for Partitioned Global Address Space Languages.” In this keynote she discussed the issues in developing programming models for large-scale parallel machines and clusters, and how PGAS languages compare to languages emerging from the DARPA HPCS program.She also presented compiler analysis and optimi- tion techniques developed in the context of UPC and Titanium source-to-source compilers for parallel program and communication optimizations.