1. Record Nr. UNISA996465923503316

Titolo	Algorithms and Architectures for Parallel Processing [[electronic resource]] : 10th International Conference, ICA3PP 2010, Busan, Korea, May 21-23, 2010. Workshops, Part II / / edited by Sang-Soo Yeo, Jong Hyuk Park, Laurence Tianruo Yang, Ching-Hsien Hsu
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2010
ISBN	1-280-38665-7 9786613564573 3-642-13136-0
Edizione	[1st ed. 2010.]
Descrizione fisica	1 online resource (XXX, 468 p. 234 illus.)
Collana	Theoretical Computer Science and General Issues, , 2512-2029 ; ; 6082
Disciplina	003.3
Soggetti	Computer systems Algorithms Artificial intelligence Software engineering Information storage and retrieval systems Computer science Computer System Implementation Artificial Intelligence Software Engineering Information Storage and Retrieval Theory of Computation
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	The 2010 International Symposium on Frontiers of Parallel and Distributed Computing (FPDC 2010) -- Efficient Grid on the OTIS-Arrangment Network -- Single Thread Program Parallelism with Dataflow Abstracting Thread -- Parallel Programming on a Soft-Core Based Multi-core System -- Dynamic Resource Tuning for Flexible Core Chip Multiprocessors -- Ensuring Confidentiality and Integrity of Multimedia Data on Multi-core Platforms -- A Paradigm for Processing

Network Protocols in Parallel -- Real-Time Task Scheduling on Heterogeneous Two-Processor Systems -- A Grid Based System for Closure Computation and Online Service -- A Multiple Grid Resource Broker with Monitoring and Information Services -- Design Methodologies of Workload Management through Code Migration in Distributed Desktop Computing Grids -- Dynamic Dependent Tasks Assignment for Grid Computing -- Implementation of a Heuristic Network Bandwidth Measurement for Grid Computing Environments -- An Efficient Circuit–Switched Broadcasting in Star Graph -- Parallel Domain Decomposition Methods for High-Order Finite Element Solutions of the Helmholtz Problem -- Self-Organizing Neural Grove and Its Distributed Performance -- A Massively Parallel Hardware for Modular Exponentiations Using the m-ary Method -- Emulation of Object-Based Storage Devices by a Virtual Machine -- Balanced Multi-process Parallel Algorithm for Chemical Compound Inference with Given Path Frequencies -- Harnessing Clusters for High Performance Computation of Gene Expression Microarray Comparative Analysis -- Semantic Access Control for Corporate Mobile Devices -- A New Visual Simulation Tool for Performance Evaluation of MANET Routing Protocols -- A Web Service Composition Algorithm Based on Global QoS Optimizing with MOCACO -- Experiences Gained from Building a Services-Based Distributed Operating System -- Quick Forwarding of Queries to Relevant Peers in a Hierarchical P2P File Search System -- iCTPH: An Approach to Publish and Lookup CTPH Digests in Chord -- Toward a Framework for Cloud Security -- Cluster-Fault-Tolerant Routing in Burnt Pancake Graphs -- Edge-Bipancyclicity of All Conditionally Faulty Hypercubes -- The 2010 International Workshop on High Performance Computing Technologies and Applications (HPCTA 2010) -- Accelerating Euler Equations Numerical Solver on Graphics Processing Units -- An Improved Parallel MEMS Processing-Level Simulation Implementation Using Graphic Processing Unit -- Solving Burgers' Equation Using Multithreading and GPU -- Support for OpenMP Tasks on Cell Architecture -- A Novel Algorithm for Faults Acquiring and Locating on Fiber Optic Cable Line -- A Parallel Distributed Algorithm for the Permutation Flow Shop Scheduling Problem -- A Self-Adaptive Load Balancing Strategy for P2P Grids -- Embedding Algorithms for Star, Bubble-Sort, Rotator-Faber-Moore, and Pancake Graphs -- Performance Estimation of Generalized Statistical Smoothing to Inverse Halftoning Based on the MTF Function of Human Eyes -- Power Improvement Using Block-Based Loop Buffer with Innermost Loop Control -- An Efficient Pipelined Architecture for Fast Competitive Learning -- Merging Data Records on EREW PRAM -- The 2010 International Workshop on Multicore and Multithreaded Architecture and Algorithms (M2A2 2010) -- Performance Modeling of Multishift QR Algorithms for the Parallel Solution of Symmetric Tridiagonal Eigenvalue Problems -- A Parallel Solution of Large-Scale Heat Equation Based on Distributed Memory Hierarchy System -- A New Metric for On-Line Scheduling and Placement in Reconfigurable Computing Systems -- Test Data Compression Using Four-Coded and Sparse Storage for Testing Embedded Core -- Extending a Multicore Multithread Simulator to Model Power-Aware Hard Real-Time Systems -- Real-Time Linux Framework for Designing Parallel Mobile Robotic Applications.

Sommario/riassunto

It is our great pleasure to present the proceedings of the symposia and workshops on parallel and distributed computing and applications associated with the ICA3PP 2010 conference. These symposia and workshops provide vibrant opportunities for researchers and industry practitioners to share their research experience, original research

results and practical development experiences in the new challenging research areas of parallel and distributed computing technologies and applications. It was the first time that the ICA3PP conference series added symposia and wo- shops to its program in order to provide a wide range of topics that extend beyond the main conferences. The goal was to provide a better coverage of emerging research areas and also forums for focused and stimulating discussions. With this objective in mind, we selected three workshops to accompany the ICA3PP 2010 conference: • FPDC 2010, the 2010 International Symposium on Frontiers of Parallel and Distributed Computing • HPCTA 2010, the 2010 International Workshop on High-Performance Computing, Technologies and Applications • M2A 2010, the 2010 International Workshop on Multicore and Mul- threaded Architectures and Algorithms Each of the symposia / workshops focused on a particular theme and complemented the spectrum of the main conference. All papers published in the workshops proce- ings were selected by the Program Committee on the basis of referee reports. Each paper was reviewed by independent referees who judged the papers for originality, quality, contribution, presentation and consistency with the theme of the workshops.

2. Record Nr. UNINA9910147236903321

Titolo	IEEE Standard VHDL Language Reference Manual
Pubbl/distr/stampa	[Place of publication not identified], : IEEE, 2002
ISBN	0-7381-3248-9
Descrizione fisica	1 online resource
Disciplina	621.3819
Soggetti	VHDL (Computer hardware description language) - Standards VHDL (Computer hardware description language) Computer hardware description languages Engineering - Computer programs
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Sommario/riassunto	VHSIC Hardware Description Language (VHDL) is defined. VHDL is a formal notation intended for use in all phases of the creation of electronic systems. Because it is both machine readable and human readable, it supports the development, verification, synthesis, and testing of hardware designs; the communication of hardware design data; and the maintenance, modification, and procurement of hardware. Its primary audiences are the implementors of tools supporting the language and the advanced users of the language. Keywords: computer languages, electronic systems, hardware, hardware design, VHDL.