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Nota di contenuto	Invited Keynote 1 -- Technology Trends and Adaptive Computing -- Architectural Frameworks -- Prototyping Framework for Reconfigurable Processors -- An Emulator for Exploring RaPiD Configurable Computing Architectures -- Place and Route 1 -- A New Placement Method for Direct Mapping into LUT-Based FPGAs -- fGREP - Fast Generic Routing Demand Estimation for Placed FPGA Circuits -- Architecture -- Macrocell Architectures for Product Term Embedded Memory Arrays -- Gigahertz Reconfigurable Computing Using SiGe HBT BiCMOS FPGAs --

Memory Synthesis for FPGA-Based Reconfigurable Computers -- DSP 1 -- Implementing a Hidden Markov Model Speech Recognition System in Programmable Logic -- Implementation of (Normalised) RLS Lattice on Virtex -- Accelerating Matrix Product on Reconfigurable Hardware for Signal Processing -- Synthesis -- Static Profile-Driven Compilation for FPGAs -- Synthesizing RTL Hardware from Java Byte Codes -- PuMA++: From Behavioral Specification to Multi-FPGA-Prototype -- Encryption -- Secure Configuration of Field Programmable Gate Arrays -- Single-Chip FPGA Implementation of the Advanced Encryption Standard Algorithm -- JBits™ Implementations of the Advanced Encryption Standard (Rijndael) -- Runtime Recon.guration 1 -- Task-Parallel Programming of Reconfigurable Systems -- Chip-Based Reconfigurable Task Management -- Configuration Caching and Swapping -- Graphics and Vision -- Multiple Stereo Matching Using an Extended Architecture -- Implementation of a NURBS to Bézier Conversor with Constant Latency -- Reconfigurable Frame-Grabber for Real-Time Automated Visual Inspection (RT-AVI) Systems -- Invited Keynote 2 -- Processing Models for the Next Generation Network -- Place and Route 2 -- Tightly Integrated Placement and Routing for FPGAs -- Gambit: A Tool for the Simultaneous Placement and Detailed Routing of Gate-Arrays -- Networking -- Reconfigurable Router Modules Using Network Protocol Wrappers -- Development of a Design Framework for Platform-Independent Networked Reconfiguration of Software and Hardware -- Processor Interaction -- The MOLEN ??-Coded Processor -- Run-Time Optimized Reconfiguration Using Instruction Forecasting -- CRISP: A Template for Reconfigurable Instruction Set Processors -- Applications -- Evaluation of an FPGA Implementation of the Discrete Element Method -- Run-Time Performance Optimization of an FPGA-Based Deduction Engine for SAT Solvers -- A Reconfigurable Embedded Input Device for Kinetically Challenged Persons -- Methodology 1 -- Bubble Partitioning for LUT-Based Sequential Circuits -- Rapid Construction of Partial Configuration Datastreams from High-Level Constructs Using JBits -- Placing, Routing, and Editing Virtual FPGAs -- DSP 2 -- Virtex Implementation of Pipelined Adaptive LMS Predictor in Electronic Support Measures Receiver -- A Music Synthesizer on FPGA -- Motivation from a Full-Rate Specific Design to a DSP Core Approach for GSM Vocoders -- Loops and Systolic -- Loop Tiling for Reconfigurable Accelerators -- The Systolic Ring: A Dynamically Reconfigurable Architecture for Embedded Systems -- A n-Bit Reconfigurable Scalar Quantiser -- Image Processing -- Real Time Morphological Image Contrast Enhancement in Virtex FPGA -- Demonstrating Real-time JPEG Image Compression-Decompression using Standard Component IP Cores on a Programmable Logic based Platform for DSP and Image Processing -- Design and Implementation of an Accelerated Gabor Filter Bank Using Parallel Hardware -- Invited Keynote 3 -- The Evolution of Programmable Logic: Past, Present, and Future Predictions -- Runtime Reconfiguration 2 -- Dynamically Reconfigurable Cores -- Reconfigurable Breakpoints for Co-debug -- Faults -- Using Design-Level Scan to Improve FPGA Design Observability and Controllability for Functional Verification -- FPGA-Based Fault Injection Techniques for Fast Evaluation of Fault Tolerance in VLSI Circuits -- Methodology 2 -- A Generic Library for Adaptive Computing Environments -- Generative Development System for FPGA essors with Active Components -- Compilation Increasing the Scheduling Scope for Multi-memory-FPGA-Based Custom Computing Machines -- System Level Tools for DSP in FPGAs -- Arithmetic -- Parameterized Function Evaluation for FPGAs -- Efficient Constant Coefficient Multiplication Using Advanced FPGA Architectures -- A Digit-Serial Structure for Reconfigurable Multipliers