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Synthesized RTL Designs and Its Integration with a High-Level Synthesis Tool -- Combined Formal Post- and Presynthesis Verification in High Level Synthesis -- Formalization and Proof of a Solution to the PCI 2.1 Bus Transaction Ordering Problem -- A Performance Study of BDD-Based Model Checking -- Symbolic Model Checking Visualization -- Input Elimination and Abstraction in Model Checking -- Symbolic Simulation of the JEM1 Microprocessor -- Symbolic Simulation: An ACL2 Approach -- Verification of Data-Insensitive Circuits: An In-Order-Retirement Case Study -- Combining Symbolic Model Checking with Uninterpreted Functions for Out-of-Order Processor Verification -- Formally Verifying Data and Control with Weak Reachability Invariants -- Generalized Reversible Rules -- An Assume-Guarantee Rule for Checking Simulation -- Three Approaches to Hardware Verification: HOL, MDG, and VIS Compared -- An Instruction Set Process Calculus -- Techniques for Implicit State Enumeration of EFSMs -- Model Checking on Product Structures -- BDDNOW: A Parallel BDD Package -- Model Checking VHDL with CV -- Alexandria: A Tool for Hierarchical Verification -- PV: An Explicit Enumeration Model-Checker.