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Nota di contenuto	The Era of Multi-core Chips -A Fresh Look on Software Challenges -- Streaming Networks for Coordinating Data-Parallel Programs (Position Statement) -- Implementations of Square-Root and Exponential Functions for Large FPGAs -- Using Branch Prediction Information for Near-Optimal I-Cache Leakage -- Scientific Computing Applications on the Imagine Stream Processor -- Enhancing Last-Level Cache Performance by Block Bypassing and Early Miss Determination -- A

Study of the Performance Potential for Dynamic Instruction Hints Selection -- Reorganizing UNIX for Reliability -- Critical-Task Anticipation Scheduling Algorithm for Heterogeneous and Grid Computing -- Processor Directed Dynamic Page Policy -- Static WCET Analysis Based Compiler-Directed DVS Energy Optimization in Real-Time Applications -- A Study on Transformation of Self-similar Processes with Arbitrary Marginal Distributions -- ?TC – An Intermediate Language for Programming Chip Multiprocessors -- Functional Unit Chaining: A Runtime Adaptive Architecture for Reducing Bypass Delays -- Trace-Based Data Cache Leakage Reduction at Link Time -- Parallelizing User-Defined and Implicit Reductions Globally on Multiprocessors -- Overload Protection for Commodity Network Appliances -- An Integrated Temporal Partitioning and Mapping Framework for Handling Custom Instructions on a Reconfigurable Functional Unit -- A High Performance Simulator System for a Multiprocessor System Based on a Multi-way Cluster -- Hardware Budget and Runtime System for Data-Driven Multithreaded Chip Multiprocessor -- Combining Wireless Sensor Network with Grid for Intelligent City Traffic -- A Novel Processor Architecture for Real-Time Control -- A 0-1 Integer Linear Programming Based Approach for Global Locality Optimizations -- Design and Analysis of Low Power Image Filters Toward Defect-Resilient Embedded Memories for Multimedia SoCs -- Entropy Throttling: A Physical Approach for Maximizing Packet Mobility in Interconnection Networks -- Design of an Efficient Flexible Architecture for Color Image Enhancement -- Hypercube Communications on Optical Chordal Ring Networks with Chord Length of Three -- PMPS(3): A Performance Model of Parallel Systems -- Issues and Support for Dynamic Register Allocation -- A Heterogeneous Multi-core Processor Architecture for High Performance Computing -- Reducing the Branch Power Cost in Embedded Processors Through Static Scheduling, Profiling and SuperBlock Formation -- Fault-Free Pairwise Independent Hamiltonian Paths on Faulty Hypercubes -- Constructing Node-Disjoint Paths in Enhanced Pyramid Networks -- Striping Cache: A Global Cache for Striped Network File System -- DTuplesHPC: Distributed Tuple Space for Desktop High Performance Computing -- The Algorithm and Circuit Design of a 400MHz 16-Bit Hybrid Multiplier -- Live Range Aware Cache Architecture -- The Challenges of Efficient Code-Generation for Massively Parallel Architectures -- Reliable Systolic Computing Through Redundancy -- A Diversity-Controllable Genetic Algorithm for Optimal Fused Traffic Planning on Sensor Networks -- A Context-Switch Reduction Heuristic for Power-Aware Off-Line Scheduling -- On the Reliability of Drowsy Instruction Caches -- Design of a Reconfigurable Cryptographic Engine -- Enhancing ICOUNT2.8 Fetch Policy with Better Fairness for SMT Processors -- The New BCD Subtractor and Its Reversible Logic Implementation -- Power-Efficient Microkernel of Embedded Operating System on Chip -- Understanding Prediction Limits Through Unbiased Branches -- Bandwidth Optimization of the EMCI for a High Performance 32-bit DSP -- Research on Petersen Graphs and Hyper-cubes Connected Interconnection Networks -- Cycle Period Analysis and Optimization of Timed Circuits -- Acceleration Techniques for Chip-Multiprocessor Simulator Debug -- A DDL–Based Software Architecture Model -- Branch Behavior Characterization for Multimedia Applications -- Optimization and Evaluating of StreamYGX2 on MASA Stream Processor -- SecureTorrent: A Security Framework for File Swarming -- Register Allocation on Stream Processor with Local Register File -- A Self-reconfigurable System-on-Chip Architecture for Satellite On-Board Computer Maintenance -- Compile-Time Thread

Distinguishment Algorithm on VIM-Based Architecture -- Designing a Coarse-Grained Reconfigurable Architecture Using Loop Self-Pipelining -- Low-Power Data Cache Architecture by Address Range Reconfiguration for Multimedia Applications -- Automatic Synthesis of Interface Circuits from Simplified IP Interface Protocols -- An Architectural Leakage Power Reduction Method for Instruction Cache in Ultra Deep Submicron Microprocessors -- An Efficient Approach to Energy Saving in Microcontrollers.

Sommario/riassunto

On behalf of all of the people involved in the program selection, the program committee members as well as numerous other reviewers, we are both relieved and pleased to present you with the proceedings of the 2006 Asia-Pacific Computer Systems Architecture Conference (ACSAC 2006), which is being hosted in Shanghai on September 6–8, 2006. This is the 11th in a series of conferences, which started life in Australia, as the computer architecture component of the Australian Computer Science Week. In 1999 it ventured away from its roots for the first time, and the fourth Australasian Computer Architecture Conference was held in the beautiful city of Sails (Auckland, New Zealand). Perhaps it was because of a lack of any other computer architecture conference in Asia or just the attraction of traveling to the Southern Hemisphere but the conference became increasingly international during the subsequent three years and also changed its name to include Computer Systems Architecture, reflecting more the scope of the conference, which embraces both architectural and systems issues. In 2003, the conference again ventured offshore to reflect its constituency and since then has been held in Japan in the beautiful city of Aizu-Wakamatsu, followed by Beijing and Singapore. This year it again returns to China and next year will move to Korea for the first time, where it will be organized by the Korea University.