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Nota di contenuto	Portable pipeline synthesis for FCCMs -- Performance-directed technology mapping for LUT-based FPGAs — What role do decomposition and covering play? -- A framework for developing parametrised FPGA libraries -- FACT: Co-evaluation environment for FPGA architecture and CAD system -- An universal CLA adder generator for SRAM-based FPGAs -- An emulation system of the

WASMII: A data driven computer on a virtual hardware -- Costum computing machines vs. Hardware/Software Co-Design: From a globalized point of view -- The design of a coprocessor board using Xilinx's XC6200 FPGA — An experience report -- RACE: Reconfigurable and adaptive computing environment -- Computing 2-D DFTs using FPGAs -- CAPpartx: Computer aided prototyping partitioning for Xilinx FPGAs, a hierarchical partitioning tool for rapid prototyping -- Architectural synthesis and efficient circuit implementation for field programmable gate arrays -- RaPiD — Reconfigurable pipelined datapath -- Solving satisfiability problems on FPGAs -- FPGA implementation of the block-matching algorithm for motion estimation in image coding -- Parallel CRC computation in FPGAs -- Coherent demodulation with FPGAs -- The Trianus system and its application to custom computing -- Logic synthesis for FPGAs using a mixed exclusive-/inclusive-OR form -- Flexible codesign target architecture for early prototyping of CMIST systems -- Attempt-1: A reconfigurable multiprocessor testbed -- A slow motion engine for the analysis of FPGA-based prototypes -- Implementing reconfigurable datapaths in FPGAs for adaptive filter design -- A fast constant coefficient multiplier for the XC6200 -- Key issues for user acceptance of FPGA design tools -- Reconfigurable DSP demonstrators for the development of spacecraft payload processors -- Reconfigurable logic based fibre channel network card with sub 2 ?s raw latency -- An asynchronous transfer mode (ATM) stream demultiplexer and switch -- Optically reconfigurable FPGAs: Is this a future trend? -- CCSimP — An instruction-level costum-configurable processor for FPLDs -- Architectural synthesis techniques for dynamically reconfigurable logic -- Fast reconfigurable crossbar switching in FPGAs -- Growable FPGA macro generator -- Architectural strategies for implementing an image processing algorithm on XC6000 FPGA -- A virtual hardware operating system for the Xilinx XC6200 -- An experimental programmable environment for prototyping digital circuits -- Migration from schematic-based designs to a VHDL synthesis environment -- ASIC design and FPGA design: A unified design methodology applied to different technologies -- FIR filtering with FPGAs using quadrature sigma-delta modulation encoding -- A new FPGA technology mapping approach by cluster merging -- An EPLD based transient recorder for simulation of video signal processing devices in a VHDL environment close to system level conditions -- Convolutional error decoding with FPGAs -- Metastability characteristics testing for programmable logic design -- Implementing ?? modulator prototype designs on an FPGA -- Design of a VME parameterized library for FPGAs -- Development of a telephone answering machine in a lab — FPGAs in Education -- FPGA design migration: Some remarks -- Concurrent design of hardware/software dedicated systems -- The implementation of a field programmable logic based co-processor for the acceleration of discrete event simulators -- Computing weight distributions of binary linear block codes on a CCM.

Sommario/riassunto

This book constitutes the refereed proceedings of the 6th International Workshop of Field-Programmable Logic and Applications, FPL '96, held in Darmstadt, Germany, in September 1996. The 37 revised full papers presented in the book are selected from 82 submissions originating from 27 countries; also included are 13 high-quality poster presentations. The book is divided into topical sections on high-level design, new software and hardware development tools, custom computers, applications, hardware/software co-design, AISC emulators, vendor session, industrial applications and experiences, reconfiguration aspects, CAD user experiences, and miscellaneous.