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Nota di contenuto	<p>Program verification using HOL-UNITY -- Graph model of LAMBDA in higher order logic -- Mechanizing a programming logic for the concurrent programming language microSR in HOL -- Reasoning with the formal definition of standard ML in HOL -- HOL-ML -- Structure and behaviour in hardware verification -- Degrees of formality in shallow embedding hardware description languages in HOL -- A functional approach for formalizing regular hardware structures -- A proof development system for the HOL theorem prover -- A HOL package for reasoning about relations defined by mutual induction -- A broader class of trees for recursive type definitions for HOL -- Some theorems we should prove -- Using PVS to prove some theorems of David Parnas -- Extending the HOL theorem prover with a computer algebra system to reason about the reals -- The HOL-Voss system: Model-checking inside a general-purpose theorem-prover -- Linking Higher Order Logic to a VLSI CAD system -- Alternative proof procedures for finite-state machines in higher-order logic -- A formalization of abstraction in LAMBDA -- Report on the UCD microcoded Viper verification project -- Verification of the Tamarack-3 microprocessor in a hybrid verification environment -- Abstraction techniques for modeling real-world interface chips -- Implementing a methodology for formally verifying RISC processors in HOL -- Domain theory in HOL -- Predicates, temporal logic, and simulations -- Formalization of variables access constraints to support compositionality of liveness properties -- The semantics of statecharts in HOL -- Value-passing CCS in HOL -- TPS: An interactive and automatic tool for proving theorems of type theory -- Modelling bit vectors in HOL: The word library -- Eliminating higher-order quantifiers to obtain decision procedures for hardware verification -- Toward a super duper hardware tactic -- A mechanisation of name-carrying syntax up to alpha-conversion -- A HOL decision procedure for elementary real algebra -- AC unification in HOL90 -- Server-process restrictiveness in HOL -- Safety in railway signalling data: A behavioural analysis -- On the style of mechanical proving -- From abstract data types to shift registers: -- Verification in higher order logic of mutual exclusion algorithm -- Using Isabelle to prove simple theorems.</p>
Sommario/riassunto	<p>This volume constitutes the refereed proceedings of the 1993 Higher-Order Logic User's Group Workshop, held at the University of British Columbia in August 1993. The workshop was sponsored by the Centre for Integrated Computer System Research. It was the sixth in the series of annual international workshops dedicated to the topic of Higher-Order Logic theorem proving, its usage in the HOL system, and its applications. The volume contains 40 papers, including an invited paper by David Parnas, McMaster University, Canada, entitled "Some theorems we should prove".</p>