1. Record Nr. UNISA996465790003316

Titolo	Correct Hardware Design and Verification Methods [[electronic resource]] : 12th IFIP WG 10.5 Advanced Research Working Conference, CHARME 2003, L'Aquila, Italy, October 21-24, 2003, Proceedings / / edited by Daniel Geist, Enrico Tronci
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2003
ISBN	3-540-39724-8
Edizione	[1st ed. 2003.]
Descrizione fisica	1 online resource (XII, 432 p.)
Collana	Lecture Notes in Computer Science, , 0302-9743 ; ; 2860
Disciplina	621.395
Soggetti	Computers Computer hardware Computer logic Software engineering Mathematical logic Artificial intelligence Theory of Computation Computer Hardware Logics and Meanings of Programs Software Engineering Mathematical Logic and Formal Languages Artificial Intelligence
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Invited Talks -- What Is beyond the RTL Horizon for Microprocessor and System Design? -- The Charme of Abstract Entities -- Tutorial -- The PSL/Sugar Specification Language A Language for all Seasons -- Software Verification -- Finding Regularity: Describing and Analysing Circuits That Are Not Quite Regular -- Predicate Abstraction with Minimum Predicates -- Efficient Symbolic Model Checking of Software Using Partial Disjunctive Partitioning -- Processor Verification -- Instantiating Uninterpreted Functional Units and Memory System:

Functional Verification of the VAMP -- A Hazards-Based Correctness Statement for Pipelined Circuits -- Analyzing the Intel Itanium Memory Ordering Rules Using Logic Programming and SAT -- Automata Based Methods -- On Complementing Nondeterministic Büchi Automata -- Coverage Metrics for Formal Verification -- “More Deterministic” vs. “Smaller” Büchi Automata for Efficient LTL Model Checking -- Short Papers 1 -- An Optimized Symbolic Bounded Model Checking Engine -- Constrained Symbolic Simulation with Mathematica and ACL2 -- Semi-formal Verification of Memory Systems by Symbolic Simulation -- CTL May Be Ambiguous When Model Checking Moore Machines -- Specification Methods -- Reasoning about GSTE Assertion Graphs -- Towards Diagrammability and Efficiency in Event Sequence Languages -- Executing the Formal Semantics of the Accellera Property Specification Language by Mechanised Theorem Proving -- Protocol Verification -- On Combining Symmetry Reduction and Symbolic Representation for Efficient Model Checking -- On the Correctness of an Intrusion-Tolerant Group Communication Protocol -- Exact and Efficient Verification of Parameterized Cache Coherence Protocols -- Short Papers 2 -- Design and Implementation of an Abstract Interpreter for VHDL -- A Programming Language Based Analysis of Operand Forwarding -- Integrating RAM and Disk Based Verification within the Mur? Verifier -- Design and Verification of CoreConnectTM IP Using Esterel -- Theorem Proving -- Inductive Assertions and Operational Semantics -- A Compositional Theory of Refinement for Branching Time -- Linear and Nonlinear Arithmetic in ACL2 -- Bounded Model Checking -- Efficient Distributed SAT and SAT-Based Distributed Bounded Model Checking -- Convergence Testing in Term-Level Bounded Model Checking -- The ROBDD Size of Simple CNF Formulas -- Model Checking and Application -- Efficient Hybrid Reachability Analysis for Asynchronous Concurrent Systems -- Finite Horizon Analysis of Markov Chains with the Mur? Verifier -- Improved Symbolic Verification Using Partitioning Techniques.