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Nota di contenuto	Memory Technology -- A 64Mbit Mesochronous Hybrid Wave Pipelined Multibank DRAM Macro -- Software Controlled Reconfigurable On-chip Memory for High Performance Computing -- Processor and Memory Architecture -- Content-Based Prefetching: Initial Results -- Memory System Support for Dynamic Cache Line Assembly -- Adaptively Mapping Code in an Intelligent Memory Architecture -- Applications and Operating Systems -- The Characterization of Data Intensive Memory Workloads on Distributed PIM Systems? -- Memory

Management in a PIM-Based Architecture -- Compiler Technology -- Exploiting On-chip Memory Bandwidth in the VIRAM Compiler -- FlexCache: A Framework for Flexible Compiler Generated Data Caching -- Poster Session -- Aggressive Memory-Aware Compilation -- Energy/Performance Design of Memory Hierarchies for Processor-in-Memory Chips? -- SAGE: A New Analysis and Optimization System for FlexRAM Architecture -- Performance/Energy Efficiency of Variable Line-Size Caches for Intelligent Memory Systems -- The DIVA Emulator: Accelerating Architecture Studies for PIM-Based Systems -- Compiler-Directed Cache Line Size Adaptivity ? -- Summary of Question/Answer Sessions for Workshop Presentations.

Sommario/riassunto

We are pleased to present this collection of papers from the Second Workshop on Intelligent Memory Systems. Increasing die densities and inter chip communication costs continue to fuel interest in intelligent memory systems. Since the First Workshop on Mixing Logic and DRAM in 1997, technologies and systems for computation in memory have developed quickly. The focus of this workshop was to bring together researchers from academia and industry to discuss recent progress and future goals. The program committee selected 8 papers and 6 poster session abstracts from 29 submissions for inclusion in the workshop. Four to five members of the program committee reviewed each submission and their reviews were used to numerically rank them and guide the selection process. We believe that the resulting program is of the highest quality and interest possible. The selected papers cover a wide range of research topics such as circuit technology, processor and memory system architecture, compilers, operating systems, and applications. They also present a mix of mature projects, work in progress, and new research ideas. The workshop also included two invited talks. Dr. Subramanian Iyer (IBM Microelectronics) provided an overview of embedded memory technology and its potential. Dr. Mark Snir (IBM Research) presented the Blue Gene, an aggressive supercomputer system based on intelligent memory technology.