1. Record Nr. UNINA990000075720403321

Autore	La Cour, Jens Lassen
Titolo	Theorie der Wechselstrome / Von J. L. La Cour und O. S. Bragstad
Pubbl/distr/stampa	Berlin : J. Springer, 1910
Edizione	[2. vollstandig umgearbeitete Auf.]
Descrizione fisica	XIII, 922 p. : ill. ; 24 cm
Collana	Die Wechselstromtechnik ; 1
Disciplina	621.313 3
Locazione	FINAG
Collocazione	23 18 B 17
Lingua di pubblicazione	Italiano
Formato	Materiale a stampa
Livello bibliografico	Monografia

2. Record Nr. UNISA996465783103316

Titolo	Intelligent Memory Systems [[electronic resource]] : Second International Workshop, IMS 2000, Cambridge, MA, USA, November 12, 2000. Revised Papers / / edited by Frederic T. Chong, Christoforos Kozyrakis, Mark Oskin
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2001
ISBN	3-540-44570-6
Edizione	[1st ed. 2001.]
Descrizione fisica	1 online resource (VIII, 200 p.)
Collana	Lecture Notes in Computer Science, , 0302-9743 ; ; 2107
Disciplina	005.4/35
Soggetti	Artificial intelligence Computer engineering Computer memory systems Computer organization Operating systems (Computers) Computer logic Artificial Intelligence Computer Engineering Memory Structures Computer Systems Organization and Communication Networks

	Operating Systems Logics and Meanings of Programs
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di contenuto	Memory Technology -- A 64Mbit Mesochronous Hybrid Wave Pipelined Multibank DRAM Macro -- Software Controlled Reconfigurable On-chip Memory for High Performance Computing -- Processor and Memory Architecture -- Content-Based Prefetching: Initial Results -- Memory System Support for Dynamic Cache Line Assembly -- Adaptively Mapping Code in an Intelligent Memory Architecture -- Applications and Operating Systems -- The Characterization of Data Intensive Memory Workloads on Distributed PIM Systems? -- Memory Management in a PIM-Based Architecture -- Compiler Technology -- Exploiting On-chip Memory Bandwidth in the VIRAM Compiler -- FlexCache: A Framework for Flexible Compiler Generated Data Caching -- Poster Session -- Aggressive Memory-Aware Compilation -- Energy/Performance Design of Memory Hierarchies for Processor-in-Memory Chips? -- SAGE: A New Analysis and Optimization System for FlexRAM Architecture -- Performance/Energy Efficiency of Variable Line-Size Caches for Intelligent Memory Systems -- The DIVA Emulator: Accelerating Architecture Studies for PIM-Based Systems -- Compiler-Directed Cache Line Size Adaptivity ? -- Summary of Question/Answer Sessions for Workshop Presentations.
Sommario/riassunto	We are pleased to present this collection of papers from the Second Workshop on Intelligent Memory Systems. Increasing die densities and inter chip communication costs continue to fuel interest in intelligent memory systems. Since the First Workshop on Mixing Logic and DRAM in 1997, technologies and systems for computation in memory have developed quickly. The focus of this workshop was to bring together researchers from academia and industry to discuss recent progress and future goals. The program committee selected 8 papers and 6 poster session abstracts from 29 submissions for inclusion in the workshop. Four to five members of the program committee reviewed each submission and their reviews were used to numerically rank them and guide the selection process. We believe that the resulting program is of the highest quality and interest possible. The selected papers cover a wide range of research topics such as circuit technology, processor and memory system architecture, compilers, operating systems, and applications. They also present a mix of mature projects, work in progress, and new research ideas. The workshop also included two invited talks. Dr. Subramanian Iyer (IBM Microelectronics) provided an overview of embedded memory technology and its potential. Dr. Mark Snir (IBM Research) presented the Blue Gene, an aggressive supercomputer system based on intelligent memory technology.