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| | Note generali | Includes index. |
| | Nota di contenuto | Architecture -- A Fast Scheme to Investigate Thermal-Aware Scheduling Policy for Multicore Processors -- Dealing with Traffic-Area Trade-Off in Direct Coherence Protocols for Many-Core CMPs -- An Efficient Lightweight Shared Cache Design for Chip Multiprocessors -- A Novel Cache Organization for Tiled Chip Multiprocessor -- A Performance Model for Run-Time Reconfigurable Hardware Accelerator -- SPMTM: A Novel ScratchPad Memory Based Hybrid Nested Transactional Memory Framework -- Implementation of Rotation Invariant Multi-View Face Detection on FPGA -- The Design and Evaluation of a Selective Way Based Trace Cache -- A Fine-Grained Pipelined Implementation for Large-Scale Matrix Inversion on FPGA -- L1 Collective Cache: Managing Shared Data for Chip Multiprocessors -- Graphical Processing Unit -- Efficient Multiplication of Polynomials on Graphics Hardware -- Performance Optimization Strategies of High Performance Computing on GPU -- A Practical Approach of Curved Ray Prestack Kirchhoff Time Migration on GPGPU -- GCSim: A GPU-Based Trace-Driven Simulator for Multi-level Cache -- A Hybrid Parallel Signature Matching Model for Network Security Applications Using SIMD GPU -- Grid -- HPVZ: A High Performance Virtual Computing |

Environment for Super Computers -- High Performance Support of Lustre over Customized HSNI for HPC -- ViroLab Security and Virtual Organization Infrastructure -- E2EDSM: An Edge-to-Edge Data Service Model for Mass Streaming Media Transmission -- Grid Scheduling -- Iso-Level CAFT: How to Tackle the Combination of Communication Overhead Reduction and Fault Tolerance Scheduling -- MaGate Simulator: A Simulation Environment for a Decentralized Grid Scheduler -- Mobile Applications -- A Distributed Shared Memory Architecture for Occasionally Connected Mobile Environments -- Time-Adaptive Vertical Handoff Triggering Methods for Heterogeneous Systems -- Energy-Saving Topology Control for Heterogeneous Ad Hoc Networks -- Parallel Applications -- Computational Performance of a Parallelized Three-Dimensional High-Order Spectral Element Toolbox -- Research on Evaluation of Parallelization on an Embedded Multicore Platform -- MapReduce-Based Pattern Finding Algorithm Applied in Motif Detection for Prescription Compatibility Network -- Parallelization of the LEMan Code with MPI and OpenMP -- The Recursive Dual-Net and Its Applications -- Parallelization Strategies for Mixed Regular-Irregular Applications on Multicore-Systems -- Performance Improvement of Multimedia Kernels by Alleviating Overhead Instructions on SIMD Devices -- Large Matrix Multiplication on a Novel Heterogeneous Parallel DSP Architecture -- Implementing Fast Packet Filters by Software Pipelining on x86 Processors -- Parallel Libraries -- OSL: Optimized Bulk Synchronous Parallel Skeletons on Distributed Arrays -- Performance -- Evaluating SPLASH-2 Applications Using MapReduce -- MPTD: A Scalable and Flexible Performance Prediction Framework for Parallel Systems.

| Sommario/riassunto | This book constitutes the refereed proceedings of the 8th International Workshop on Advanced Parallel Processing Technologies, APPT 2009, held in Rapperswil, Switzerland, in August 2009. The 36 revised full papers presented were carefully reviewed and selected from 76 submissions. All current aspects in parallel and distributed computing are addressed ranging from hardware and software issues to algorithmic aspects and advanced applications. The papers are organized in topical sections on architecture, graphical processing unit, grid, grid scheduling, mobile application, parallel application, parallel libraries and performance. |