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Titolo	High Performance Embedded Architectures and Compilers [[electronic resource]] : First International Conference, HiPEAC 2005, Barcelona, Spain, November 17-18, 2005, Proceedings // edited by Tom Conte, Nacho Navarro, Wen-mei W. Hwu, Mateo Valero, Theo Ungerer
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Soggetti	Computer arithmetic and logic units Computer systems Compilers (Computer programs) Computer input-output equipment Logic design Microprocessors Computer architecture Arithmetic and Logic Structures Computer System Implementation Compilers and Interpreters Input/Output and Data Communications Logic Design Processor Architectures
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Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Invited Program -- Keynote 1: Using EEMBC Benchmarks to Understand Processor Behavior in Embedded Applications -- Keynote 2: The Chip-Multiprocessing Paradigm Shift: Opportunities and Challenges -- Software Defined Radio – A High Performance Embedded Challenge -- I Analysis and Evaluation Techniques -- A Practical Method for Quickly Evaluating Program Optimizations -- Efficient Sampling Startup for Sampled Processor Simulation -- Enhancing Network Processor

Simulation Speed with Statistical Input Sampling -- II Novel Memory and Interconnect Architectures -- Power Aware External Bus Arbitration for System-on-a-Chip Embedded Systems -- Beyond Basic Region Caching: Specializing Cache Structures for High Performance and Energy Conservation -- Streaming Sparse Matrix Compression/Decompression -- XAMM: A High-Performance Automatic Memory Management System with Memory-Constrained Designs -- III Security Architecture -- Memory-Centric Security Architecture -- A Novel Batch Rekeying Processor Architecture for Secure Multicast Key Management -- Arc3D: A 3D Obfuscation Architecture -- IV Novel Compiler and Runtime Techniques -- Dynamic Code Region (DCR) Based Program Phase Tracking and Prediction for Dynamic Optimizations -- Induction Variable Analysis with Delayed Abstractions -- Garbage Collection Hints -- V DomainSpecificArchitectures -- Exploiting a Computation Reuse Cache to Reduce Energy in Network Processors -- Dynamic Evolution of Congestion Trees: Analysis and Impact on Switch Architecture -- A Single (Unified) Shader GPU Microarchitecture for Embedded Systems -- A Low-Power DSP-Enhanced 32-Bit EISC Processor.

Sommario/riassunto

As Chairmen of HiPEAC 2005, we have the pleasure of welcoming you to the proceedings of the first international conference promoted by the HiPEAC Network of Excellence. During the last year, HiPEAC has been building its clusters of researchers in computer architecture and advanced compiler techniques for embedded and high-performance computers. Recently, the Summer School has been the seed for a fruitful collaboration of renowned international faculty and young researchers from 23 countries with fresh new ideas. Now, the conference promises to be among the premier forums for discussion and debate on these research topics.

The prestige of a symposium is mainly determined by the quality of its technical program. This first program lived up to our high expectations, thanks to the large number of strong submissions. The Program Committee received a total of 84 submissions; only 17 were selected for presentation as full-length papers and another one as an invited paper. Each paper was rigorously reviewed by three Program Committee members and at least one external referee. Many reviewers spent a great amount of effort to provide detailed feedback. In many cases, such feedback along with constructive shepherding resulted in dramatic improvement in the quality of accepted papers. The names of the Program Committee members and the referees are listed in the proceedings. The net result of this team effort is that the symposium proceedings include outstanding contributions by authors from nine countries in three continents. In addition to paper presentations, this first HiPEAC conference featured two keynotes delivered by prominent researchers from industry and academia.
