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| Nota di contenuto | Keynote Speech -- Architectural Challenges for the Next Decade Integrated Platforms -- Gate-Level Modeling and Design -- Analysis of High-Speed Logic Families -- Low Voltage, Double-Edge-Triggered Flip Flop -- A Genetic Bus Encoding Technique for Power Optimization of Embedded Systems -- State Encoding for Low-Power FSMs in FPGA -- Low Level Modeling and Characterization -- Reduced Leverage of Dual Supply Voltages in Ultra Deep Submicron Technologies -- A Compact Charge-Based Crosstalk Induced Delay Model for Submicronic CMOS |

Gates -- CMOS Gate Sizing under Delay Constraint -- Process Characterisation for Low VTH and Low Power Design -- Power and Energy Consumption of CMOS Circuits: Measurement Methods and Experimental Results -- Interconnect Modeling and Optimization -- Effects of Temperature in Deep-Submicron Global Interconnect Optimization -- Interconnect Parasitic Extraction Tool for Radio-Frequency Integrated Circuits -- Estimation of Crosstalk Noise for On-Chip Buses -- A Block-Based Approach for SoC Global Interconnect Electrical Parameters Characterization -- Interconnect Driven Low Power High-Level Synthesis -- Asynchronous Techniques -- Bridging Clock Domains by Synchronizing the Mice in the Mousetrap -- Power-Consumption Reduction in Asynchronous Circuits Using Delay Path Unequalization -- New GALS Technique for Datapath Architectures -- Power/Area Tradeoffs in 1-of-M Parallel-Prefix Asynchronous Adders -- Static Implementation of QDI Asynchronous Primitives -- Keynote Speech -- The Emergence of Design for Energy Efficiency: An EDA Perspective -- Industrial Session -- The Most Complete Mixed-Signal Simulation Solution with ADVance MS -- Signal Integrity and Power Supply Network Analysis of Deep SubMicron Chips -- Power Management in Synopsys Galaxy Design Platform -- Open Multimedia Platform for Next-Generation Mobile Devices -- RTL Power Modeling and Memory Optimisation -- Statistical Power Estimation of Behavioral Descriptions -- A Statistical Power Model for Non-synthetic RTL Operators -- Energy Efficient Register Renaming -- Stand-by Power Reduction for Storage Circuits -- A Unified Framework for Power-Aware Design of Embedded Systems -- High-Level Modeling -- A Flexible Framework for Fast Multi-objective Design Space Exploration of Embedded Systems -- High-Level Area and Current Estimation -- Switching Activity Estimation in Non-linear Architectures -- Instruction Level Energy Modeling for Pipelined Processors -- Power Estimation Approach of Dynamic Data Storage on a Hardware Software Boundary Level -- Power Efficient Technologies and Designs -- An Adiabatic Charge Pump Based Charge Recycling Design Style -- Reduction of the Energy Consumption in Adiabatic Gates by Optimal Transistor Sizing -- Low-Power Response Time Accelerator with Full Resolution for LCD Panel -- Memory Compaction and Power Optimization for Wavelet-Based Coders -- Design Space Exploration and Trade-Offs in Analog Amplifier Design -- Keynote Speech -- Power and Timing Driven Physical Design Automation -- Communication Modeling and Design -- Analysis of Energy Consumed by Secure Session Negotiation Protocols in Wireless Networks -- Remote Power Control of Wireless Network Interfaces -- Architecture-Driven Voltage Scaling for High-Throughput Turbo-Decoders -- A Fully Digital Numerical-Controlled-Oscillator -- Low Power Issues in Processors and Multimedia -- Energy Optimization of High-Performance Circuits -- Instruction Buffering Exploration for Low Energy Embedded Processors -- Power-Aware Branch Predictor Update for High-Performance Processors -- Power Optimization Methodology for Multimedia Applications Implementation on Reconfigurable Platforms -- High-Level Algorithmic Complexity Analysis for the Implementation of a Motion-JPEG2000 Encoder -- Poster Session 1 -- Metric Definition for Circuit Speed Optimization -- Optical versus Electrical Interconnections for Clock Distribution Networks in New VLSI Technologies -- An Asynchronous Viterbi Decoder for Low-Power Applications -- Analysis of the Contribution of Interconnect Effects in Energy Dissipation of VLSI Circuits -- A New Hybrid CBL-CMOS Cell for Optimum Noise/Power Application -- Computational Delay Models to Estimate the Delay of Floating Cubes in CMOS Circuits -- Poster Session 2 -- A Practical ASIC Methodology for

Flexible Clock Tree Synthesis with Routing Blockages -- Frequent Value Cache for Low-Power Asynchronous Dual-Rail Bus -- Reducing Static Energy of Cache Memories via Prediction-Table-Less Way Prediction -- A Bottom-Up Approach to On-Chip Signal Integrity -- Advanced Cell Modeling Techniques Based on Polynomial Expressions -- RTL-Based Signal Statistics Calculation Facilitates Low Power Design Approaches -- Poster Session 3 -- Data Dependences Critical Path Evaluation at C/C++ System Level Description -- A Hardware/Software Partitioning and Scheduling Approach for Embedded Systems with Low-Power and High Performance Requirements -- Consideration of Control System and Memory Contributions in Practical Resource-Constrained Scheduling for Low Power -- Low-Power Cache with Successive Tag Comparison Algorithm -- FPGA Architecture Design and Toolset for Logic Implementation -- Bit-Level Allocation for Low Power in Behavioural High-Level Synthesis.

Sommario/riassunto

Welcome to the proceedings of PATMOS 2003. This was the 13th in a series of international workshops held in several locations in Europe. Over the years, PATMOS has gained recognition as one of the major European events devoted to power and timing aspects of integrated circuit and system design. Despite its signi?cant growth and development, PATMOS can still be considered as a very informal forum, featuring high-level scienti?c presentations together with open discussions and panel sessions in a free and relaxed environment. This year, PATMOS took place in Turin, Italy, organized by the Politecnico di Torino, with technical co-sponsorship from the IEEE Circuits and Systems Society and the generous support of the European Commission, as well as that of several industrial sponsors, including BullDAST, Cadence, Mentor Graphics, STMicroelectronics, and Synopsys. The objective of the PATMOS workshop is to provide a forum to discuss and investigate the emerging problems in methodologies and tools for the design of new generations of integrated circuits and systems. A major emphasis of the technical program is on speed and low-power aspects, with particular regard to modeling, characterization, design, and architectures.