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Nota di contenuto	Heterogeneous Reconfigurable System for Adaptive Particle Filters in Real-Time Applications -- Hardware Acceleration of Genetic Sequence Alignment -- An FPGA Acceleration for the Kd-tree Search in Photon Mapping -- SEU Resilience of DES, AES in SRAM-based FPGA -- An Architecture for IPv6 Lookup Using Parallel Index Generation Units -- Hardware Index to Set Partition Converter -- Teaching SoC Using Video Games to Improve Student Engagement -- Parameterized Design and Evaluation of Bandwidth Compressor for Floating-Point Data Streams in FPGA-based Custom Computing -- Hardware Acceleration of Matrix Multiplication Over Small Prime Finite Fields -- Flexible Design of a Modular Simultaneous Exponentiation Core for Embedded Platforms -- Architecture for Transparent Binary Acceleration of Loops with Memory Accesses -- Parametric Optimization of Reconfigurable Designs using Machine Learning -- Fast Template-based Heterogeneous MPSoC Synthesis on FPGA -- Hierarchical and Multiple Switching NoC with

Floorplan based Adaptability -- Performance Analysis And Optimization of High Density Tree-Based 3D Multilevel FPGA.

Sommario/riassunto

This book constitutes the thoroughly refereed conference proceedings of the 9th International Symposium on Reconfigurable Computing: Architectures, Tools and Applications, ARC 2013, held in Los Angeles, CA, USA, in March 2013. The 28 revised papers presented, consisting of 20 full papers and 11 poster papers were carefully selected from 41 submissions. The topics covered are applications, arithmetic, design optimization for FPGAs, architectures, place and routing.