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Nota di contenuto	Applications -- Implementation of Realtime and Highspeed Phase Detector on FPGA -- Case Study: Implementation of a Virtual Instrument on a Dynamically Reconfigurable Platform -- Configurable Embedded Core for Controlling Electro-Mechanical Systems -- Evaluation of a Locomotion Algorithm for Worm-Like Robots on FPGA-Embedded Processors -- Dynamic Partial Reconfigurable FIR Filter Design -- Event-Driven Simulation Engine for Spiking Neural Networks on a Chip -- Towards an Optimal Implementation of MLP in FPGA -- Power -- Energy Consumption for Transport of Control Information on a Segmented Software-Controlled Communication Architecture --

Quality Driven Dynamic Low Power Reconfiguration of Handhelds -- An Efficient Estimation Method of Dynamic Power Dissipation on VLSI Interconnects -- Image Processing -- Highly Paralellized Architecture for Image Motion Estimation -- Design Exploration of a Video Pre-processor for an FPGA Based SoC -- QUKU: A Fast Run Time Reconfigurable Platform for Image Edge Detection -- Applications of Small-Scale Reconfigurability to Graphics Processors -- An Embedded Multi-camera System for Simultaneous Localization and Mapping -- Performance/Cost Trade-Off Evaluation for the DCT Implementation on the Dynamically Reconfigurable Processor -- Trigonometric Computing Embedded in a Dynamically Reconfigurable CORDIC System-on-Chip -- Handel-C Design Enhancement for FPGA-Based DV Decoder -- Run-Time Resources Management on Coarse Grained, Packet-Switching Reconfigurable Architecture: A Case Study Through the APACHES' Platform -- A New VLSI Architecture of Lifting-Based DWT -- Architecture Based on FPGA's for Real-Time Image Processing -- Real Time Image Processing on a Portable Aid Device for Low Vision Patients -- General Purpose Real-Time Image Segmentation System -- Organization and Architecture -- Implementation of LPM Address Generators on FPGAs -- Self Reconfiguring EPIC Soft Core Processors -- Constant Complexity Management of 2D HW Multitasking in Run-Time Reconfigurable FPGAs -- Area/Performance Improvement of NoC Architectures -- Implementation of Inner Product Architecture for Increased Flexibility in Bitwidths of Input Array -- A Flexible Multi-port Caching Scheme for Reconfigurable Platforms -- Enhancing a Reconfigurable Instruction Set Processor with Partial Predication and Virtual Opcode Support -- A Reconfigurable Data Cache for Adaptive Processors -- The Emergence of Non-von Neumann Processors -- Scheduling Reconfiguration Activities of Run-Time Reconfigurable RTOS Using an Aperiodic Task Server -- A New Approach to Assess Defragmentation Strategies in Dynamically Reconfigurable FPGAs -- A 1,632 Gate-Count Zero-Overhead Dynamic Optically Reconfigurable Gate Array VLSI -- PISC: Polymorphic Instruction Set Computers -- Networks and Communication -- Generic Network Interfaces for Plug and Play NoC Based Architecture -- Providing QoS Guarantees in a NoC by Virtual Channel Reservation -- Efficient Floating-Point Implementation of High-Order (N)LMS Adaptive Filters in FPGA -- A Reconfigurable Architecture for MIMO Square Root Decoder -- Security -- Time-Memory Trade-Off Attack on FPGA Platforms: UNIX Password Cracking -- Updates on the Security of FPGAs Against Power Analysis Attacks -- Reconfigurable Modular Arithmetic Logic Unit for High-Performance Public-Key Cryptosystems -- FPGA Implementation of a GF(2 m) Tate Pairing Architecture -- Iterative Modular Division over GF (2 m): Novel Algorithm and Implementations on FPGA -- Mobile Fingerprint Identification Using a Hardware Accelerated Biometric Service Provider -- UNITE: Uniform Hardware-Based Network Intrusion deTection Engine -- Tools -- Impact of Loop Unrolling on Area, Throughput and Clock Frequency in ROCCC: C to VHDL Compiler for FPGAs -- Automatic Compilation Framework for Bloom Filter Based Intrusion Detection -- A Basic Data Routing Model for a Coarse-Grain Reconfigurable Hardware -- Hardware and a Tool Chain for ADRES -- Integrating Custom Instruction Specifications into C Development Processes -- A Compiler-Oriented Architecture Description for Reconfigurable Systems -- Dynamic Instruction Merging and a Reconfigurable Array: Dataflow Execution with Software Compatibility -- High-Level Synthesis Using SPARK and Systolic Array -- Super Semi-systolic Array-Based Application-Specific PLD Architecture.

Sommario/riassunto

1 The International Workshop on Recon?gurable Computing (ARC)

started in 2005 in Algarve, Portugal. The major motivation was to create an event where on-going research e?orts as well as more elaborated, interesting and hi- quality work on applied recon?gurable computing could be presented and d- cussed. Over the last couple of years recon?gurable computing has become a we- known and established research area producing interesting as well as important results in both general and embedded computing systems. It is also getting more and more interest from industry which is attracted by the (design and development) ?exibility as well as the performance improvements that can be expected from this technology. As recon? gurablecomputing has blurred the gap between software and hardware, some even speak of a radical new programming paradigm opening a new realm of unseen applications and opportunities. The logo of the ARC workshop is the Nonius, a measurement instrument used in the Portuguese period of discoveries that was invented by Pedro Nunes, a Portuguesemathematician. As the logo suggests,the main motto of ARC is to help to navigate the world of recon?gurable computing. Driven by this motto, we hope ARC contributes to solid advances on recon? gurable computing.