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Titolo	Formal Methods in Computer-Aided Design [[electronic resource]] : First International Conference, FMCAD '96, Palo Alto, CA, USA, November 6 - 8, 1996, Proceedings / / edited by Mandayam Srivas, Albert Camilleri
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Descrizione fisica	1 online resource (X, 478 p.)
Collana	Lecture Notes in Computer Science, , 0302-9743 ; ; 1166
Disciplina	621.39/2
Soggetti	Computer-aided engineering Computers Computer engineering Computer hardware Computer logic Mathematical logic Computer-Aided Engineering (CAD, CAE) and Design Theory of Computation Computer Engineering Computer Hardware Logics and Meanings of Programs Mathematical Logic and Formal Languages
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di contenuto	The need for formal methods for integrated circuit design -- Verification of all circuits in a floating-point unit using word-level model checking -- *BMDs can delay the use of theorem proving for verifying arithmetic assembly instructions -- Modular verification of multipliers -- Verification of IEEE compliant subtractive division algorithms -- Hierarchical verification of two-dimensional high-speed multiplication in PVS: A case study -- Experiments in automating hardware verification using inductive proof planning -- Verifying

nondeterministic implementations of deterministic systems -- A methodology for processor implementation verification -- Coverage-directed test generation using symbolic techniques -- Self-consistency checking -- Inverting the abstraction mapping: A methodology for hardware verification -- Validity checking for combinations of theories with equality -- A unified approach for combining different formalisms for hardware verification -- Verification using uninterpreted functions and finite instantiations -- Formal verification of the Island Tunnel Controller using Multiway Decision Graphs -- VIS -- PVS: Combining specification, proof checking, and model checking -- HOL Light: A tutorial introduction -- A tutorial on digital design derivation using DRS -- ACL2 theorems about commercial microprocessors -- Formal synthesis in circuit design — A classification and survey -- Formal specification and verification of VHDL -- Specification of control flow properties for verification of synthesized VHDL designs -- An algebraic model of correctness for superscalar microprocessors -- Mechanically checking a lemma used in an automatic verification tool -- Automatic generation of invariants in processor verification -- A brief study of BDD package performance -- Local encoding transformations for optimizing OBDD-representations of finite state machines -- Decomposition techniques for efficient ROBDD construction -- BDDs vs. Zero-Suppressed BDDs: for CTL symbolic model checking of Petri nets -- HDL-based integration of formal methods and CAD tools in the PREVAIL environment.

Sommario/riassunto

This book constitutes the refereed proceedings of the First International Conference on Formal Methods in Computer-Aided Design, FMCAD '96, held in Palo Alto, California, USA, in November 1996. The 25 revised full papers presented were selected from a total of 65 submissions; also included are three invited survey papers and four tutorial contributions. The volume covers all relevant formal aspects of work in computer-aided systems design, including verification, synthesis, and testing.