

1. Record Nr.	UNISA996465510303316
Titolo	High Performance Embedded Architectures and Compilers [[electronic resource]] : 5th International Conference, HiPEAC 2010, Pisa, Italy, January 25-27, 2010, Proceedings / / edited by Yale N. Patt, Pierfrancesco Foglia, Evelyn Duesterwald, Paolo Faraboschi, Xavier Martorell
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Descrizione fisica	1 online resource (XIII, 370 p.)
Collana	Theoretical Computer Science and General Issues, , 2512-2029 ; ; 5952
Disciplina	005.4/53
Soggetti	Computer programming Computer arithmetic and logic units Microprocessors Computer architecture Computer input-output equipment Logic design Computer networks Programming Techniques Arithmetic and Logic Structures Processor Architectures Input/Output and Data Communications Logic Design Computer Communication Networks
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Invited Program -- Embedded Systems as Datacenters -- Larrabee: A Many-Core Intel Architecture for Visual Computing -- Architectural Support for Concurrency -- Remote Store Programming -- Low-Overhead, High-Speed Multi-core Barrier Synchronization -- Improving

Performance by Reducing Aborts in Hardware Transactional Memory --
Energy and Throughput Efficient Transactional Memory for Embedded
Multicore Systems -- Compilation and Runtime Systems -- Split
Register Allocation: Linear Complexity Without the Performance Penalty
-- Trace-Based Data Layout Optimizations for Multi-core Processors --
Buffer Sizing for Self-timed Stream Programs on Heterogeneous
Distributed Memory Multiprocessors -- Automatically Tuning Sparse
Matrix-Vector Multiplication for GPU Architectures -- Reconfigurable
and Customized Architectures -- Virtual Ways: Efficient Coherence for
Architecturally Visible Storage in Automatic Instruction Set Extensions
-- Accelerating XML Query Matching through Custom Stack Generation
on FPGAs -- An Application-Aware Load Balancing Strategy for Network
Processors -- Memory-Aware Application Mapping on Coarse-Grained
Reconfigurable Arrays -- Multicore Efficiency, Reliability, and Power --
Maestro: Orchestrating Lifetime Reliability in Chip Multiprocessors --
Combining Locality Analysis with Online Proactive Job Co-scheduling in
Chip Multiprocessors -- RELOCATE: Register File Local Access Pattern
Redistribution Mechanism for Power and Thermal Management in Out-
of-Order Embedded Processor -- Performance and Power Aware CMP
Thread Allocation Modeling -- Memory Organization and Optimization
-- Multi-level Hardware Prefetching Using Low Complexity Delta
Correlating Prediction Tables with Partial Matching -- Scalable Shared-
Cache Management by Containing Thrashing Workloads -- SRP:
Symbiotic Resource Partitioning of the Memory Hierarchy in CMPs --
DIEF: An Accurate Interference Feedback Mechanism for Chip
Multiprocessor Memory Systems -- Programming and Analysis of
Accelerators -- Tagged Procedure Calls (TPC): Efficient Runtime
Support for Task-Based Parallelism on the Cell Processor -- Analysis of
Task Offloading for Accelerators -- Offload – Automating Code
Migration to Heterogeneous Multicore Systems -- Computer Generation
of Efficient Software Viterbi Decoders.

Sommario/riassunto

This book constitutes the refereed proceedings of the 5th International Conference on High Performance Embedded Architectures and Compilers, HiPEAC 2010, held in Pisa, Italy, in January 2010. The 23 revised full papers presented together with the abstracts of 2 invited keynote addresses were carefully reviewed and selected from 94 submissions. The papers are organized in topical sections on architectural support for concurrency; compilation and runtime systems; reconfigurable and customized architectures; multicore efficiency, reliability, and power; memory organization and optimization; and programming and analysis of accelerators.

2. Record Nr.	UNISALENTO991003216069707536
Autore	Plinius Secundus, Gaius
Titolo	Histoire naturelle : livre 35. / Pline l'Ancien ; texte établi, traduit et commenté par Jean-Michel Croisille
Pubbl/distr/stampa	Paris : Les Belles Lettres, 1983
ISBN	2251011854
Descrizione fisica	327 p. (36-126 doppie) ; 20 cm.
Collana	Collection des Universités de France. Série latine
Altri autori (Persone)	Croisille, Jean-Michel
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Soggetti	Plinio Secondo, Gaio - Naturalis historia
Lingua di pubblicazione	Francese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Testo latino a fronte.