

1. Record Nr.	UNINA990000039310403321
Autore	Heise, F.
Titolo	Traite theorique et pratique des explosifs : destine aux exploitants des mines et de carrières et comprenant une etude speciale sur la question du grisou et des poussières dans les mines de charbon / F. Heise ; traduit de l'allemand et adapté par J. Aubrun
Pubbl/distr/stampa	Paris-Liege : Ch. Beranger, 1907
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Autore	Sharp Richard
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Soggetti	Electronics Microelectronics Computer hardware Microprocessors Software engineering Programming languages (Electronic computers) Computer logic Electronics and Microelectronics, Instrumentation Computer Hardware Processor Architectures Software Engineering Programming Languages, Compilers, Interpreters Logics and Meanings of Programs
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Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	1. Introduction -- 1. Introduction -- 2. Related Work -- 3. The SAFL Language -- 4. Soft Scheduling -- 5. High-Level Synthesis of SAFL -- 6. Analysis and Optimisation of Intermediate Code -- 7. Dealing with I/O -- 8. Combining Behaviour and Structure -- 9. Transformation of SAFL Specifications -- 10. Case Study -- 11. Conclusions and Further Work.
Sommario/riassunto	In the mid 1960s, when a single chip contained an average of 50

transistors, Gordon Moore observed that integrated circuits were doubling in complexity every year. In an influential article published by Electronics Magazine in 1965, Moore predicted that this trend would continue for the next 10 years. Despite being criticized for its “unrealistic optimism,” Moore’s prediction has remained valid for far longer than even he imagined: today, chips built using state-of-the-art techniques typically contain several million transistors. The advances in fabrication technology that have supported Moore’s law for four decades have fuelled the computer revolution. However, this exponential increase in transistor density poses new design challenges to engineers and computer scientists alike. New techniques for managing complexity must be developed if circuits are to take full advantage of the vast numbers of transistors available. In this monograph we investigate both (i) the design of high-level languages for hardware description, and (ii) techniques involved in translating these high-level languages to silicon. We propose SAFL, a first-order functional language designed specifically for behavioral hardware description, and describe the implementation of its associated silicon compiler. We show that the high-level properties of SAFL allow one to exploit program analyses and optimizations that are not employed in existing synthesis systems. Furthermore, since SAFL fully abstracts the low-level details of the implementation technology, we show how it can be compiled to a range of different design styles including fully synchronous design and globally asynchronous locally synchronous (GALS) circuits.
