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Sommario/riassunto	In the mid 1960s, when a single chip contained an average of 50

transistors, Gordon Moore observed that integrated circuits were doubling in complexity every year. In an in?uential article published by Electronics Magazine in 1965, Moore predicted that this trend would continue for the next 10 years. Despite being criticized for its “unrealistic optimism,” Moore’s prediction has remained valid for far longer than even he imagined: today, chips built using state-- the-art techniques typically contain several million transistors. The advances in fabrication technology that have supported Moore’s law for four decades have fuelled the computer revolution. However,this exponential increase in transistor density poses new design challenges to engineers and computer scientists alike. New techniques for managing complexity must be developed if circuits are to take full advantage of the vast numbers of transistors available. In this monograph we investigate both (i) the design of high-level languages for hardware description, and (ii) techniques involved in translating these hi- level languages to silicon. We propose SAFL, a ?rst-order functional language designedspeci? callyforbehavioralhardwaredescription,anddescribetheimp- mentation of its associated silicon compiler. We show that the high-level pr- erties of SAFL allow one to exploit program analyses and optimizations that are not employed in existing synthesis systems. Furthermore, since SAFL fully abstracts the low-leveldetails of the implementation technology, we show how it can be compiled to a range of di?erent design styles including fully synchronous design and globally asynchronous locally synchronous (GALS) circuits.