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Nota di contenuto	Keynote Address I -- Some Real Observations on Virtual Machines -- Session 1A: Cache and Memory -- Replica Victim Caching to Improve Reliability of In-Cache Replication -- Efficient Victim Mechanism on Sector Cache Organization -- Cache Behavior Analysis of a Compiler-Assisted Cache Replacement Policy -- Modeling the Cache Behavior of Codes with Arbitrary Data-Dependent Conditional Structures -- Session 1B: Reconfigurable and Embedded Architectures -- A Configurable System-on-Chip Architecture for Embedded Devices -- An Auto-adaptative Reconfigurable Architecture for the Control -- Enhancing the Memory Performance of Embedded Systems with the Flexible Sequential and Random Access Memory -- Heuristic Algorithm for

Reducing Mapping Sets of Hardware-Software Partitioning in Reconfigurable System -- Session 2A: Processor Architecture and Design I -- Architecture Design of a High-Performance 32-Bit Fixed-Point DSP -- TengYue-1: A High Performance Embedded SoC -- A Fault-Tolerant Single-Chip Multiprocessor -- Session 2B: Power and Energy Management -- Initial Experiences with Dreamy Memory and the RAMpage Memory Hierarchy -- dDVS: An Efficient Dynamic Voltage Scaling Algorithm Based on the Differential of CPU Utilization -- High Performance Microprocessor Design Methods Exploiting Information Locality and Data Redundancy for Lower Area Cost and Power Consumption -- Session 3A: Processor Architecture and Design II -- Dynamic Reallocation of Functional Units in Superscalar Processors -- Multiple-Dimension Scalable Adaptive Stream Architecture -- Impact of Register-Cache Bandwidth Variation on Processor Performance -- Session 3B: Compiler and Operating System Issues -- Exploiting Free Execution Slots on EPIC Processors for Efficient and Accurate Runtime Profiling -- Continuous Adaptive Object-Code Re-optimization Framework -- Initial Evaluation of a User-Level Device Driver Framework -- Keynote Address II -- A Generation Ahead of Microprocessor: Where Software Can Drive uArchitecture To? -- Session 4A: Application-Specific Systems -- A Cost-Effective Supersampling for Full Scene AntiAliasing -- A Simple Architectural Enhancement for Fast and Flexible Elliptic Curve Cryptography over Binary Finite Fields GF(2 m) -- Scalable Design Framework for JPEG2000 System Architecture -- Real-Time Three Dimensional Vision -- Session 4B: Interconnection Networks -- A Router Architecture for QoS Capable Clusters -- Optimal Scheduling Algorithms in WDM Optical Interconnects with Limited Range Wavelength Conversion Capability -- Comparative Evaluation of Adaptive and Deterministic Routing in the OTIS-Hypercube -- A Two-Level On-Chip Bus System Based on Multiplexers -- Keynote Address III -- Make Computers Cheaper and Simpler -- Session 5A: Prediction Techniques -- A Low Power Branch Predictor to Selectively Access the BTB -- Static Techniques to Improve Power Efficiency of Branch Predictors -- Choice Predictor for Free -- Performance Impact of Different Data Value Predictors -- Session 5B: Parallel Architecture and Programming -- Heterogeneous Networks of Workstations -- Finding High Performance Solution in Reconfigurable Mesh-Connected VLSI Arrays -- Order Independent Transparency for Image Composition Parallel Rendering Machines -- An Authorization Architecture Oriented to Engineering and Scientific Computation in Grid Environments -- Session 6A: Microarchitecture Design and Evaluations -- Validating Word-Oriented Processors for Bit and Multi-word Operations -- Dynamic Fetch Engine for Simultaneous Multithreaded Processors -- A Novel Rename Register Architecture and Performance Analysis -- Session 6B: Memory and I/O Systems -- A New Hierarchy Cache Scheme Using RAM and Pagefile -- An Object-Oriented Data Storage System on Network-Attached Object Devices -- A Scalable and Adaptive Directory Scheme for Hardware Distributed Shared Memory -- Session 7A: Potpourri -- A Compiler-Assisted On-Chip Assigned-Signature Control Flow Checking -- A Floating Point Divider Performing IEEE Rounding and Quotient Conversion in Parallel -- Efficient Buffer Allocation for Asynchronous Linear Pipelines by Design Space Localization.

Sommario/riassunto

On behalf of the program committee, we were pleased to present this year’s program for ACSAC: Asia-Paci?c Computer Systems Architecture Conference. Now in its ninth year, ACSAC continues to provide an excellent forum for researchers, educators and practitioners to come to the Asia-Paci?c region to exchange ideas on the latest developments in

computer systems architecture. This year, the paper submission and review processes were semiautomated using the free version of CyberChair. We received 152 submissions, the largest number ever. Eachpaperwasassignedatleastthree,mostlyfour,andinafewcaseseven ?ve committee members for review. All of the papers were reviewed in a t-monthperiod,
duringwhichtheprogramchairsregularlymonitoredtheprogress of the review process. When reviewers claimed inadequate expertise, additional reviewers were solicited. In the end, we received a total of 594 reviews (3.9 per paper) from committee members as well as 248 coreviewers whose names are acknowledged in the proceedings. We would like to thank all of them for their time and e?ort in providing us with such timely and high-quality reviews, some of them on extremely short notice.