1. Record Nr. UNISA996465341603316 VLSI-SoC: New Technology Enabler [[electronic resource]]: 27th IFIP Titolo WG 10.5/IEEE International Conference on Very Large Scale Integration. VLSI-SoC 2019, Cusco, Peru, October 6-9, 2019, Revised and Extended Selected Papers / / edited by Carolina Metzler, Pierre-Emmanuel Gaillardon, Giovanni De Micheli, Carlos Silva-Cardenas, Ricardo Reis Pubbl/distr/stampa Cham:,: Springer International Publishing:,: Imprint: Springer,, 2020 3-030-53273-9 **ISBN** Edizione [1st ed. 2020.] Descrizione fisica 1 online resource (XVII, 345 p. 214 illus., 129 illus. in color.) IFIP Advances in Information and Communication Technology, , 1868-Collana 4238;;586 Disciplina 621.395 Soggetti Computer organization Microprogramming Input-output equipment (Computers) Operating systems (Computers) Computer Systems Organization and Communication Networks Control Structures and Microprogramming Input/Output and Data Communications **Operating Systems** Lingua di pubblicazione Inglese **Formato** Materiale a stampa Livello bibliografico Monografia Software-Based Self-Test for Delay Faults -- On Test Generation for Nota di contenuto Microprocessors for Extended Class of Functional Faults -- Robust FinFET Schmitt Trigger Designs for Low Power Applications -- An Improved Technique for Logic Gate Susceptibility Evaluation of Single Event Transient Faults -- Process Variability Impact on the SET Response of FinFET Multi-level Design -- Efficient Soft Error Vulnerability Analysis Using Non-Intrusive Fault Injection Techniques -- A Statistical Wafer Scale Error and Redundancy Analysis Simulator --

> Hardware-enabled Secure Firmware Updates in Embedded Systems --Reliability Enhanced Digital Low-Dropout Regulator with Improved Transient Performance -- Security Aspects of Real-time MPSoCs: The

Flaws and Opportunities of Preemptive NoCs -- Offset-Compensation Systems for Multi-Gbit/s Optical Receivers -- Accelerating Inference on Binary Neural Networks with Digital RRAM Processing -- Semi- and Fully-Random Access LUTs for Smooth Functions -- A Predictive Process Design Kit for Three-Independent-Gate Field-Effect Transistors -- Exploiting Heterogeneous Mobile Architectures through a Unified Runtime Framework.

Sommario/riassunto

This book contains extended and revised versions of the best papers presented at the 27th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2019, held in Cusco, Peru, in October 2019. The 15 full papers included in this volume were carefully reviewed and selected from the 28 papers (out of 82 submissions) presented at the conference. The papers discuss the latest academic and industrial results and developments as well as future trends in the field of System-on-Chip (SoC) design, considering the challenges of nano-scale, state-of-the-art and emerging manufacturing technologies. In particular they address cutting-edge research fields like heterogeneous, neuromorphic and brain-inspired, biologically-inspired, approximate computing systems.