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Nota di contenuto	Keynotes (Abstracts) -- High-Performance Energy-Efficient Reconfigurable Accelerators/Co-processors for Tera-Scale Multi-core Microprocessors -- Process Variability and Degradation: New Frontier for Reconfigurable -- Towards Analytical Methods for FPGA Architecture Investigation -- Session 1: Architectures 1 -- Generic Systolic Array for Run-Time Scalable Cores -- Virtualization within a Parallel Array of Homogeneous Processing Units -- Feasibility Study of a Self-healing Hardware Platform -- Session 2: Applications 1 -- Application-Specific Signatures for Transactional Memory in Soft Processors -- Towards Rapid Dynamic Partial Reconfiguration in Video-

Based Driver Assistance Systems -- Parametric Encryption Hardware Design -- A Reconfigurable Implementation of the Tate Pairing Computation over GF(2 m) -- Session 3: Architectures 2 -- Application Specific FPGA Using Heterogeneous Logic Blocks -- Reconfigurable Communication Networks in a Parametric SIMD Parallel System on Chip -- A Dedicated Reconfigurable Architecture for Finite State Machines -- MEMS Dynamic Optically Reconfigurable Gate Array Usable under a Space Radiation Environment -- Session 4: Applications 2 -- An FPGA Accelerator for Hash Tree Generation in the Merkle Signature Scheme -- A Fused Hybrid Floating-Point and Fixed-Point Dot-Product for FPGAs -- Optimising Memory Bandwidth Use for Matrix-Vector Multiplication in Iterative Methods -- Design of a Financial Application Driven Multivariate Gaussian Random Number Generator for an FPGA -- Session 5: Design Tools 1 -- 3D Compaction: A Novel Blocking-Aware Algorithm for Online Hardware Task Scheduling and Placement on 2D Partially Reconfigurable Devices -- TROUTE: A Reconfigurability-Aware FPGA Router -- Space and Time Sharing of Reconfigurable Hardware for Accelerated Parallel Processing -- Routing-Aware Application Mapping Considering Steiner Points for Coarse-Grained Reconfigurable Architecture -- Session 6: Design Tools 2 -- Design Automation for Reconfigurable Interconnection Networks -- A Framework for Enabling Fault Tolerance in Reconfigurable Architectures -- QUAD – A Memory Access Pattern Analyser -- Hierarchical Loop Partitioning for Rapid Generation of Runtime Configurations -- Session 7: Applications 3 -- Reconfigurable Computing and Task Scheduling for Active Storage Service Processing -- A Reconfigurable Disparity Engine for Stereovision in Advanced Driver Assistance Systems -- A Modified Merging Approach for Datapath Configuration Time Reduction -- Posters -- Reconfigurable Computing Education in Computer Science -- Hardware Implementation of the Orbital Function for Quantum Chemistry Calculations -- Reconfigurable Polyphase Filter Bank Architecture for Spectrum Sensing -- Systolic Algorithm Mapping for Coarse Grained Reconfigurable Array Architectures -- A GMM-Based Speaker Identification System on FPGA -- An FPGA-Based Real-Time Event Sampler -- A Performance Evaluation of CUBE: One-Dimensional 512 FPGA Cluster -- An Analysis of Delay Based PUF Implementations on FPGA -- Comparison of Bit Serial Computation with Bit Parallel Computation for Reconfigurable Processor -- FPGA Implementation of QR Decomposition Using MGS Algorithm -- Memory-Centric Communication Architecture for Reconfigurable Computing -- Integrated Design Environment for Reconfigurable HPC -- Architecture-Aware Custom Instruction Generation for Reconfigurable Processors -- Cost and Performance Evaluation of a Noise Filter for Partitioning in Co-design Methodologies -- Towards a Tighter Integration of Generated and Custom-Made Hardware -- Pipelined Microprocessors Optimization and Debugging.

Sommario/riassunto

Reconfigurable computing (RC) systems have generated considerable interest in the embedded and high-performance computing communities over the past two decades, with field programmable gate arrays (FPGAs) as the leading technology at the helm of innovation in this discipline. Achieving orders of magnitude performance and power improvements using FPGAs over traditional microprocessors is not uncommon for well-suited applications. But even with two decades of research and technological advances, FPGA design still presents a substantial challenge and often necessitates hardware design expertise to exploit its true potential. Although the challenges to address the design productivity - sues are steep, the promise and the potential of the RC technology in terms of performance, power, size, and versatility

continue to attract application design engineers and RC researchers alike. The International Symposium on Applied Reconfigurable Computing (ARC) aims to bring together researchers and practitioners of RC systems with an emphasis on practical applications and design methodologies of this promising technology. This year's ARC symposium (The sixth ARC symposium) was held in Bangkok, Thailand during March 17–19, 2010, and attracted papers in three primary focus areas: RC applications, RC architectures, and RC design methodologies.