1. Record Nr. UNINA9910480910103321

Autore	Shore Cecilia M
Titolo	Individual differences in language development [[electronic resource] /] / Cecilia M. Shore
Pubbl/distr/stampa	Thousand Oaks, : SAGE, c1995
ISBN	1-322-42059-9 1-4833-2715-9 1-4522-5532-6
Descrizione fisica	1 online resource (161 p.)
Collana	Individual differences and development series ; ; v. 7
Disciplina	401 401.9 401/.9
Soggetti	Language acquisition Individual differences Electronic books.
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and indexes.
Nota di contenuto	Cover; Contents; Series Editor's Preface; Preface; Chapter 1 - Introduction: The Importance of Differences in Language Development; Chapter 2 - Characterizing the Nature of the Differences; Chapter 3 - Are There Styles of Language Development?; Chapter 4 - Explanations for Individual Differences in Language Development; Chapter 5 - Conclusions and Future Directions; References; Name Index; Subject Index; About the Author
Sommario/riassunto	Do all children learn language in the same way? Is the apparent `fast' versus `slow' learning rate among children a reflection of the individual child's approach to language acquisition? This volume explores the importance that individual differences have in language acquisition and challenges some widely held theories of linguistic development. Focusing on one- to three-year-old children, Cecilia Shore describes characteristic differences in terms of vocabulary, grammatical and phonological development. She considers whether distinctive 'styles' of language development can be def

2. Record Nr. UNISA996395960803316

Autore	Calamy Edmund <1600-1666.>
Titolo	An ansvver to the articles against Master Calamy, Master Martiall, Master Burton, Master Peters, Master Moleigne, Master Case, M. Sedgwicke, M. Evans, &c. and many other painfull divines [[electronic resource]] : who were impeached of high treason by His Majesty : first answering particularly the articles themselves, then shewing the mis-information of His Majestie by the bishops, concerning the same : expressing the great care and vigilancy of those theologians which they have and doe daily undertake with great zeale for the rooting out of popery the confounding of Rome and for the erecting the pious truth and sincerity of the holy gospel of Christ
Pubbl/distr/stampa	London, : Printed for William Bond ..., 1642
Descrizione fisica	[2], 5 p
Soggetti	Treason - England Trials (Treason) - England - 17th century Great Britain History Charles I, 1625-1649
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Attributed to Edmund Calamy. cf. BLC. Reproduction of original in Thomason Collection, British Library.
Sommario/riassunto	eebo-0158

3. Record Nr. UNINA9910144211603321

Titolo	High Performance Computing -- HiPC 2003 : 10th International Conference, Hyderabad, India, December 17-20, 2003, Proceedings / / edited by Timothy Mark Pinkston, Viktor K. Prasanna
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2003
ISBN	1-280-30655-6 9786610306558 3-540-24596-0
Edizione	[1st ed. 2003.]
Descrizione fisica	1 online resource (XX, 512 p.)
Collana	Lecture Notes in Computer Science, , 0302-9743 ; ; 2913
Disciplina	004.1/1
Soggetti	Microprocessors Software engineering Computer organization Computers Algorithms Numerical analysis Processor Architectures Software Engineering/Programming and Operating Systems Computer Systems Organization and Communication Networks Computation by Abstract Devices Algorithm Analysis and Problem Complexity Numeric Computing
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references at the end of each chapters and index.
Nota di contenuto	Keynote Address -- Life’s Duplicities: Sex, Death, and Valis -- Session I – Performance Issues and Power-Aware Architectures -- Performance Analysis of Blue Gene/L Using Parallel Discrete Event Simulation -- An Efficient Web Cache Replacement Policy -- Timing Issues of Operating Mode Switch in High Performance Reconfigurable Architectures -- Power-Aware Adaptive Issue Queue and Register File -- FV-MSB: A

Scheme for Reducing Transition Activity on Data Buses -- Session II – Parallel/Distributed and Network Algorithms -- A Parallel Iterative Improvement Stable Matching Algorithm -- Self-Stabilizing Distributed Algorithm for Strong Matching in a System Graph -- Parallel Data Cube Construction: Algorithms, Theoretical Analysis, and Experimental Evaluation -- Efficient Algorithm for Embedding Hypergraphs in a Cycle -- Mapping Hypercube Computations onto Partitioned Optical Passive Star Networks -- Keynote Address -- The High Performance Microprocessor in the Year 2013: What Will It Look Like? What It Won't Look Like? -- Session III – Routing in Wireless, Mobile, and Cut-Through Networks -- FROOTS – Fault Handling in Up*/Down* Routed Networks with Multiple Roots -- Admission Control for DiffServ Based Quality of Service in Cut-Through Networks -- On Shortest Path Routing Schemes for Wireless Ad Hoc Networks -- A Hierarchical Routing Method for Load-Balancing -- Ring Based Routing Schemes for Load Distribution and Throughput Improvement in Multihop Cellular, Ad hoc, and Mesh Networks -- Session IV – Scientific and Engineering Applications -- A High Performance Computing System for Medical Imaging in the Remote Operating Room -- Parallel Partitioning Techniques for Logic Minimization Using Redundancy Identification -- Parallel and Distributed Frequent Itemset Mining on Dynamic Datasets -- A Volumetric FFT for BlueGene/L -- A Nearly Linear-Time General Algorithm for Genome-Wide Bi-allele Haplotype Phasing -- Keynote Address -- Energy Aware Algorithm Design via Probabilistic Computing: From Algorithms and Models to Moore's Law and Novel (Semiconductor) Devices -- Session V – System Support in Overlay Networks, Clusters, and Grid -- Designing SANs to Support Low-Fanout Multicasts -- POMA: Prioritized Overlay Multicast in Ad Hoc Environments -- Supporting Mobile Multimedia Services with Intermittently Available Grid Resources -- Exploiting Non-blocking Remote Memory Access Communication in Scientific Benchmarks -- Session VI – Scheduling and Software Algorithms -- Scheduling Directed A-Cyclic Task Graphs on Heterogeneous Processors Using Task Duplication -- Double-Loop Feedback-Based Scheduling Approach for Distributed Real-Time Systems -- Combined Scheduling of Hard and Soft Real-Time Tasks in Multiprocessor Systems -- An Efficient Algorithm to Compute Delay Set in SPMD Programs -- Dynamic Load Balancing for I/O-Intensive Tasks on Heterogeneous Clusters -- Keynote Address -- Standards Based High Performance Computing -- Session VII – Network Design and Performance Issues -- Delay and Jitter Minimization in High Performance Internet Computing -- An Efficient Heuristic Search for Optimal Wavelength Requirement in Static WDM Optical Networks -- Slot Allocation Schemes for Delay Sensitive Traffic Support in Asynchronous Wireless Mesh Networks -- Multicriteria Network Design Using Distributed Evolutionary Algorithm -- Session VIII – Grid Applications and Architecture Support -- GridOS: Operating System Services for Grid Architectures -- Hierarchical and Declarative Security for Grid Applications -- A Middleware Substrate for Integrating Services on the Grid -- Performance Analysis of a Hybrid Overset Multi-block Application on Multiple Architectures -- Complexity Analysis of a Cache Controller for Speculative Multithreading Chip Multiprocessors -- Keynote Address -- One Chip, One Server: How Do We Exploit Its Power? -- Session IX – Performance Evaluation and Analysis -- Data Locality Optimization for Synthesis of Efficient Out-of-Core Algorithms -- Performance Evaluation of Working Set Scheme for Location Management in PCS Networks -- Parallel Performance of the Interpolation Supplemented Lattice Boltzmann Method -- Crafting Data Structures: A Study of Reference Locality in

Refinement-Based Pathfinding -- Improving Performance Analysis Using Resource Management Information -- Session X – Scheduling and Migration -- Optimizing Dynamic Dispatches through Type Invariant Region Analysis -- Thread Migration/Checkpointing for Type-Unsafe C Programs -- Web Page Characteristics-Based Scheduling -- Controlling Kernel Scheduling from User Space: An Approach to Enhancing Applications' Reactivity to I/O Events -- High-Speed Migration by Anticipative Mobility.

Sommario/riassunto

This book constitutes the refereed proceedings of the 10th International Conference on High-Performance Computing, HiPC 2003, held in Hyderabad, India in December 2003.The 48 revised full papers presented together with 5 keynote abstracts were carefully reviewed and selected from 164 submissions. The papers are organized in topical sections on performance issues and power-aware systems; distributed and network algorithms; routing in wireless, mobile, and cut-through networks; scientific and engineering applications; overlay networks, clusters, and grids; scheduling and software algorithms; network design and performance; grid applications and architecture support; performance analysis; scheduling and migration.