

1. Record Nr.	UNISA996394758903316
Titolo	Gratiae theatrales, or, A choice ternary of English plays [[electronic resource] /] / composed upon especial occasions by several ingenious persons
Pubbl/distr/stampa	London, : Printed by R.D., 1662
Descrizione fisica	[14], 57 p
Altri autori (Persone)	T. W <fl. 1662.> WatsonThomas <d. 1686.>
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	"Never before published, but now printed at the request of sundry ingenious friends." Imperfect: all after Thorny-Abbey missing. Thorny-abbey has been attributed (probably erroneously) to Thomas Watson. Reproduction of original in the Bodleian Library.
Nota di contenuto	Thorny-Abbey, or, The London maid / by T.W.--The marriage-broker, or, The pander / by M.W.--Grim the collier of Croydon, or, The devil and his dame / by I.T.
Sommario/riassunto	eebo-0014

2. Record Nr.	UNINA9911020441003321
Autore	Fleury Martin <1951->
Titolo	Pipeline processor farms : structured design for embedded parallel systems / / M. Fleury, A.C. Downton
Pubbl/distr/stampa	New York, : Wiley, 2001
ISBN	9786610264773 9781280264771 1280264772 9780471464143 0471464147 9780471224389 0471224383
Descrizione fisica	1 online resource (330 p.)
Collana	Wiley series on parallel and distributed computing
Altri autori (Persone)	DowntonA. C
Disciplina	005.2/76
Soggetti	Embedded computer systems - Programming Parallel computers - Programming
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di contenuto	Foreword; Preface; Acknowledgments; Contents; Acronyms; Part I: Introduction and Basic Concepts; 1 Introduction; 1.1 Overview; 1.2 Origins; 1.3 Amdahl's Law and Structured Parallel Design; 1.4 Introduction to PPF Systems; 1.5 Conclusions; Appendix; 2 Basic Concepts; 2.1 Pipelined Processing; 2.2 Pipeline Types; 2.3 Data Farming and Demand-based Scheduling; 2.4 Data-farm Performance Criteria; 2.5 Conclusion; Appendix; 3 PPF in Practice; 3.1 Application Overview; 3.2 Parallelization of the Postcode Recognizer; 3.3 Parallelization of the address verifier; 3.4 Meeting the Specification 3.5 ConclusionAppendix; 4 Development of PPF Applications; 4.1 Analysis Tools; 4.2 Tool Characteristics; 4.3 Development Cycle; 4.4 Conclusion; Part II: Analysis and Partitioning of Sequential Applications; 5 Initial Development of an Application; 5.1 Confidence Building; 5.2 Automatic and Semi-automatic Parallelization; 5.3 Language Proliferation; 5.4 Size of Applications; 5.5 Semi-automatic Partitioning; 5.6 Porting Code; 5.7 Checking a Decomposition; 5.8 Optimizing

Compilers; 5.9 Conclusion; 6 Graphical Simulation and Performance Analysis of PPFs; 6.1 Simulating Asynchronous Pipelines 6.2 Simulation Implementation6.3 Graphical Representation; 6.4 Display Features; 6.5 Cross-architectural Comparison; 6.6 Conclusion; 7 Template-based Implementation; 7.1 Template Design Principles; 7.2 Implementation Choices; 7.3 Parallel Logic Implementation; 7.4 Target Machine Implementation; 7.5 'NOW' Implementation for Logic Debugging; 7.6 Target Machine Implementations for Performance Tuning; 7.7 Patterns and Templates; 7.8 Conclusion; Part III: Case Studies; 8 Application Examples; 8.1 Case Study 1: H.261 Encoder; 8.2 Case Study 2: H263 Encoder/Decoder 8.3 Case Study 3: 'Eigenfaces' - Face Detection8.4 Case Study 4: Optical Flow; 8.5 Conclusion; 9 Design Studies; 9.1 Case Study 1: Karhunen-Loeve Transform (KLT); 9.2 Case Study 2: 2D- Wavelet Transform; 9.3 Case Study 3: Vector Quantization; 9.4 Conclusion; 10 Counter Examples; 10.1 Case Study 1: Large Vocabulary Continuous-Speech Recognition; 10.2 Case Study 2: Model-based Coding; 10.3 Case Study 3: Microphone Beam Array; 10.4 Conclusion; Part IV: Underlying Theory and Analysis; 11 Performance of PPFs; 11.1 Naming Conventions; 11.2 Performance Metrics; 11.3 Gathering Performance Data 11.4 Performance Prediction Equations11.5 Results; 11.6 Simulation Results; 11.7 Asynchronous Pipeline Estimate; 11.8 Ordering Constraints; 11.9 Task Scheduling; 11.10 Scheduling Results; 11.11 Conclusion; Appendix; 12 Instrumentation of Templates; 12.1 Global Time; 12.2 Processor Model; 12.3 Local Clock Requirements; 12.4 Steady-state Behavior; 12.5 Establishing a Refresh Interval; 12.6 Local Clock Adjustment; 12.7 Implementation on the Paramid; 12.8 Conclusion; Part V: Future Trends; 13 Future Trends; 13.1 Designing for Differing Embedded Hardware 13.2 Adapting to Mobile Networked Computation

Sommario/riassunto

This book outlines a methodology for the use of parallel processing in real time systems. It provides an introduction to parallel processing in general, and to embedded systems in particular. Among the embedded systems are processors in such applications as automobiles, various machinery, FPGAs (field programmable gate arrays), multimedia embedded systems such as those used in the computer game industry, and more.* Presents design and simulation tools as well as case studies.* First presentation of this material in book form.
