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| Sommario/riassunto | Reuse of test data and test structures developed for individual cores (designs) when integrated into larger integrated circuits is required for system-on-chip (SoC) tests. This standard defines language constructs sufficient to represent the context of a memory core and of the integration of that memory core into an SoC. This facilitates the development and reuse of test and repair mechanisms for memories. This standard also defines constructs that represent the test structures internal to the memory core for reuse in the creation of the tests for the logic outside the memory core. Semantic rules are defined for the language to facilitate interoperability between different entities (the memory core provider, the system integrator, and the automation tool developer) involved in the creation of an SoC. The capabilities are an extension of IEEE Std 1450.6-2005. As a result of this extension, CTL's limitations of handling memories are addressed. Keywords: core test language (CTL), IEEE 1450.6.2, memory built-in self-test (memory BIST), memory modeling, memory repair, standard test interface language (STIL), system-on-chip (SoC). |