1. **Record Nr.**   UNISA996280506403316

   Titolo   IEEE standard for a control and status registers (CSR) architecture for microcomputer buses

   Pubbl/distr/stampa New York : , : IEEE, , 2002

   Descrizione fisica 1 online resource (67 pages)

   Disciplina   004.16

   Soggetti   Microcomputers - Buses - Standards
                           Computer architecture - Standards

   Lingua di pubblicazione Inglese

   Formato   Materiale a stampa

   Livello bibliografico Monografia

   Sommario/riassunto A common bus architecture (which includes functional components - modules, nodes, and units - and their address space, transaction set, CSRs, and configuration information) suitable for both parallel and serial buses is provided in this standard. Bus bridges are enabled by the architecture, but their details are beyond its scope. Configuration information is self-administered by vendors and organizations based upon IEEE Registration Authority company_id.