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Nota di contenuto	Real-time FPGA-based architecture for bicubic interpolation: an application for digital image scaling, -- An image comparison circuit design," -- FPGA-based customizable systolic architecture for image processing applications," -- An FPGA arithmetic logic unit for computing scalar multiplication using the half-and-add method," -- Hardware signal processing unit for one-dimensional variable-length discrete wavelet transform," -- A Handel-C implementation of the back-propagation algorithm on field programmable gate arrays," -- Rapid prototyping of a self-timed ALU with FPGAs," -- FPGA implementation of a synchronous and self-timed neuroprocessor," -- On the design of two-level reconfigurable architectures," -- A secure self-reconfiguring architecture based on open-source hardware," -- Platform for intrinsic evolution of analogue neural networks," -- High quality uniform random number generation for massively parallel simulations in FPGA," -- VANNGen: a flexible CAD tool for hardware implementation of artificial neural networks," -- Quartz: a framework for correct and efficient reconfigurable design," -- Design space exploration of coarse-grain reconfigurable DSPs," -- Optimizing register binding in FPGAs using simulated annealing," -- An FPGA-based parallel sorting architecture for the Burrows Wheeler transform," -- Dynamic voting schemes to enhance evolutionary repair in reconfigurable logic devices," -- Applied VHDL training methodology, EDA framework and hardware implementation platform," -- FPGA implementation of DSVPWM modulator," -- A novel FPGA implementation of a welding control using a new bus architecture," --

On the design of an FPGA-based OFDM modulator for IEEE 802.16-2004," -- Design and implementation of an embedded microprocessor compatible with IL language in accordance to the norm IEC 61131-3," -- VHDL core for 1024-point radix-4 FFT computation," -- Hierarchical FPGA clustering based on multilevel partitioning approach to improve routability and reduce power dissipation," -- FPGA implementation of an efficient multiplier over finite fields GF(2/sup m/)," -- An FPGA-based coprocessor for the SPHINX speech recognition system: early experiences," -- Hardware/software implementation of a discrete cosine transform algorithm using SystemC.