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Sommario/riassunto	3D discrete wavelet transform (DWT) is a compute-intensive task that is usually implemented on specific architectures in many real-time medical imaging systems. In this paper, a novel area-efficient high-throughput 3D DWT architecture is proposed based on distributed arithmetic. A tap-merging technique is used to reduce the size of DA lookup tables. The proposed architectures were designed in VHDL and mapped to a Xilinx Virtex-E FPGA. The synthesis results show the proposed architecture has a low area cost and can run up to 85 MHz, which can perform a five-level 3D wavelet analysis for seven 128 times 128 times 128 volume images per second.