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Nota di contenuto	2001 IEEE International Symposium on Performance Analysis of Systems and Software [front matter] -- MASE: a novel infrastructure for detailed microarchitectural modeling -- Early design phase power/performance modeling through statistical simulation -- Performance analysis using pipeline visualization -- Implementation and evaluation of a best-effort scheduling algorithm in an embedded real-time system -- An evaluation of the POSIX trace standard implemented in RT-linux -- Cycle accurate thread timer for linux environmenthang -- About the sensitivity of the HLRC-DU protocol on diff and page sizes -- Geist: a generator for e-commerce & internet server traffic -- Performance characterization experience of multi-tier e-business systems using queuing operational analysis -- Understanding control flow transfer and its predictability in java processing -- The effects of context switching on branch predictor performance -- Estimating internal memory fragmentation for java programs under the binary buddy policy -- An evaluation of search tree techniques in the presence of caches -- Automatic memory hierarchy characterization -- Using program and user information to improve file prediction performance -- Efficient profile-based evaluation of randomising set index functions for cache memories -- Workload characterization of multithreaded java servers -- Behavior and performance of interactive multi-player game servers -- Parallel simulation of multiprocessor execution:

implementation and results for simple-scalar -- Locality-aware predictive scheduling of network processors -- Statistical usage testing applied to mobile network verification -- Balancing throughput and fairness in SMT processors -- An empirical study of the scalability aspects of instruction distribution algorithms for clustered processors -- How to compare the performance of two SMT microarchitectures -- Author index.
