1.	Record Nr.	UNISA990003702560203316
	Autore	BREYER, Yvonne Alexandra
	Titolo	Corpora in language teaching and learning : potential, evaluation, challenges / Yvonne Alexandra Breyer
	Pubbl/distr/stampa	Frankfurt am Main : Peter Lang, 2011
	ISBN	978-3-631-63041-9
	Descrizione fisica	XII, 268 p. : ill. ; 22 cm
	Collana	English corpus linguistics ; 13
	Disciplina	410.18
	Soggetti	Corpora
	Collocazione	I.8.A.101
	Lingua di pubblicazione	Inglese
	Formato	Materiale a stampa
	Livello bibliografico	Monografia

2.	Record Nr.	UNINA9910350221703321
	Autore	Wang Guilei
	Titolo	Investigation on SiGe Selective Epitaxy for Source and Drain Engineering in 22 nm CMOS Technology Node and Beyond / / by Guilei Wang
	Pubbl/distr/stampa	Singapore : , : Springer Singapore : , : Imprint : Springer, , 2019
	ISBN	981-15-0046-0
	Edizione	[1st ed. 2019.]
	Descrizione fisica	1 online resource (XVI, 115 p.)
	Collana	Springer Theses, Recognizing Outstanding Ph.D. Research, , 2190-5053
	Disciplina	537.622
	Soggetti	Semiconductors Electronic circuits Nanotechnology Circuits and Systems Nanotechnology and Microengineering
	Lingua di pubblicazione	Inglese
	Formato	Materiale a stampa
	Livello bibliografico	Monografia
	Note generali	"Doctoral thesis accepted by Chinese Academy of Sciences, Beijing, China"--Title page.
	Nota di bibliografia	Includes bibliographical references.
	Nota di contenuto	Introduction -- Strain technology of Si-based materials -- SiGe Epitaxial Growth and material characterization -- SiGe Source and Drain Integration and transistor performance investigation -- Pattern Dependency behavior of SiGe Selective Epitaxy -- Summary and final words.
	Sommario/riassunto	This thesis presents the SiGe source and drain (S/D) technology in the context of advanced CMOS, and addresses both device processing and epitaxy modelling. As the CMOS technology roadmap calls for continuously downscaling traditional transistor structures, controlling the parasitic effects of transistors, e.g. short channel effect, parasitic resistances and capacitances is becoming increasingly difficult. The emergence of these problems sparked a technological revolution, where a transition from planar to three-dimensional (3D) transistor design occurred in the 22nm technology node. The selective epitaxial growth (SEG) method has been used to deposit SiGe as stressor material in S/D regions to induce uniaxial strain in the channel region. The thesis investigates issues of process integration in IC production and concentrates on the key parameters of high-quality SiGe selective

epitaxial growth, with a special focus on its pattern dependency behavior and on key integration issues in both 2D and 3D transistor structures, the goal being to improve future applications of SiGe SEG in advanced CMOS.